# XT25F32F

## Quad IO Serial NOR Flash

## Datasheet

* Information furnished is believed to be accurate and reliable. However, XTX Technology Inc. assumes no responsibility for the consequences of use of such information or for any infringement of patents of other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent rights of XTX Technology Inc. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. XTX Technology Inc. products are not authorized for use as critical components in life support devices or systems without express written approval of XTX Technology Inc. The XTX logo is a registered trademark of XTX Technology Inc. All other names are the property of their respective own.

# Serial NOR Flash Memory

## 3.3V Multi I/O with 4KB, 32KB & 64KB Sector/Block Erase

- **32M -bit Serial Flash**
  - 4096K-byte
  - 256 bytes per programmable page
- **Support SFDP & Unique ID**
- **Standard, Dual, Quad SPI**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64k-byte
- **Advanced security Features**
  - 3*1024-Byte Security Registers With OTP Lock
- **Software/Hardware Write Protection**
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top or Bottom Block Protection
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Allows XIP(execute in place)operation**
  - High speed Read reduce overall XIP instruction fetch time
  - Continuous Read with Wrap further reduce data latency to fill up SoC cache
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40℃ to +85℃), MSL3
- **Power Consumption**
  - 0.3uA typ. power down current
- **Single Power Supply Voltage**
  - 2.7~3.6V
- **Endurance and Data Retention**
  - Minimum 100,000 Program/Erase Cycle
  - 20-year Data Retention typical
- **High Speed Clock Frequency**
  - 133MHz for fast read with 30pF load
  - Dual I/O Data transfer up to 266Mbit/s
  - Quad I/O Data transfer up to 532Mbit/s
  - Continuous Read With 8/16/32/64-byte Wrap
- **Program/Erase Speed**
  - Page Program time: 0.4ms typical
  - Sector Erase time: 50ms typical
  - Block Erase time: 0.15/0.25s typical
  - Chip Erase time: 12s typical

# CONTENTS


**1. GENERAL DESCRIPTION ..... 5**

1.1. Available Ordering OPN ..... 5
1.2. Connection Diagram ..... 6
1.3. Pin Description ..... 7
1.4. Block Diagram ..... 7

**2. MEMORY ORGANIZATION ..... 8**

**3. DEVICE OPERATION ..... 9**

**4. DATA PROTECTION ..... 11**

**5. STATUS REGISTER ..... 13**

**6. COMMANDS DESCRIPTION ..... 16**

6.1. Write Enable (WREN) (06H) ..... 19
6.2. Write Enable for Volatile Status Register (50H) ..... 19
6.3. Write Disable (WRDI) (04H) ..... 20
6.4. Read Status Register (RDSR) (05H or 35H or 15H) ..... 20
6.5. Write Status Register (WRSR) (01H or 31H or 11H) ..... 21
6.6. Read Data Bytes (READ) (03H) ..... 22
6.7. Read Data Bytes At Higher Speed (Fast Read) (0BH) ..... 22
6.8. Dual Output Fast Read (3BH) ..... 23
6.10. Dual I/O Fast Read (BBH) ..... 24
6.11. Quad Output Fast Read (6BH) ..... 26
6.12. Quad I/O Fast Read (EBH) ..... 26
6.13. Page Program (PP) (02H) ..... 28
6.14. Quad Page Program (QPP) (32H) ..... 29
6.15. Sector Erase (SE) (20H) ..... 30
6.16. 32KB Block Erase (BE) (52H) ..... 30
6.17. 64KB Block Erase (BE) (D8H) ..... 31
6.18. Chip Erase (CE) (60/C7H) ..... 32
6.19. Set Burst with Wrap (77H) ..... 33
6.20. Deep Power-Down (DP) (B9H) ..... 34
6.21. Release from Deep Power-Down and Read Device ID (RDI) (ABH) ..... 35
6.22. Read Manufacture ID/ Device ID (REMS) (90H) ..... 36
6.23. Read Serial Flash Discoverable Parameter (5AH) ..... 36
6.24. Read Unique ID(4BH) ..... 38
6.25. Read Identification (RDID) (9FH) ..... 38
6.26. Erase Security Registers (44H) ..... 39
6.27. Program Security Registers (42H) ..... 40
6.28. Read Security Registers (48H) ..... 41
6.29. Enable Reset (66H) and Reset (99H) ..... 42

**7. ELECTRICAL CHARACTERISTICS ..... 43**

7.1. Power-on Timing ..... 43
7.2. Initial Delivery State ..... 43
7.3. Latch up Characteristics ..... 43
7.4. Absolute Maximum Ratings ..... 44

7.5. CAPACITANCE MEASUREMENT CONDITION ..... 44
7.6. DC CHARACTERISTICS ..... 45
7.7. AC CHARACTERISTICS ..... 46

**8. ORDERING INFORMATION ..... 49**

**9. PACKAGE INFORMATION ..... 50**

9.1. PACKAGE SOP8 150MIL ..... 50
9.2. PACKAGE SOP8 208MIL ..... 51
9.3. PACKAGE DFN8 (2X3X0.4) MM ..... 52

**10. REVISION HISTORY ..... 53**

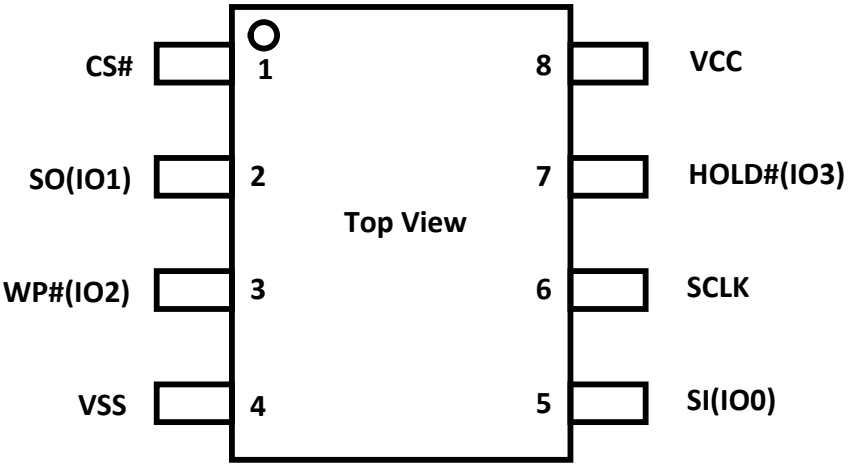
# 1. GENERAL DESCRIPTION

The XT25F32F (32M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#).

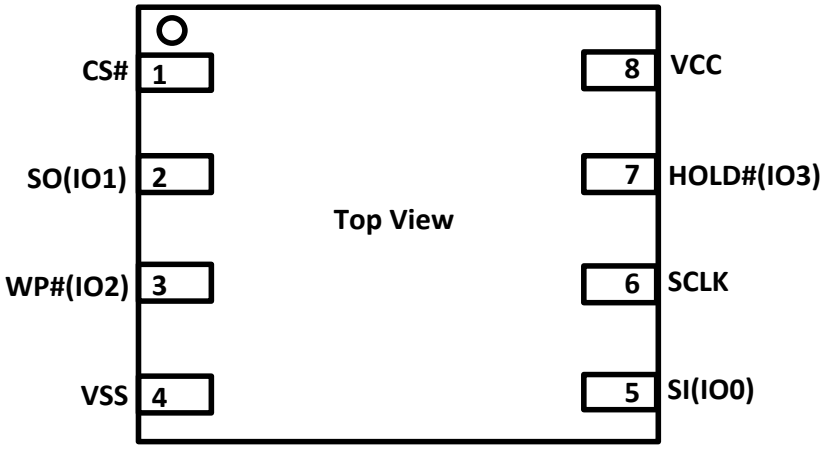
## 1.1. Available Ordering OPN

| OPN | Package Type | Package Carrier |
|---|---|---|
| XT25F32FSOIGU | SOP8 150mil | Tube |
| XT25F32FSOIGT | SOP8 150mil | Tape & Reel |
| XT25F32FSSIGU | SOP8 208mil | Tube |
| XT25F32FSSIGT | SOP8 208mil | Tape & Reel |
| XT25F32FDTIGT | DFN8 2x3x0.4mm | Tape & Reel |

## 1.2. Connection Diagram




**8-PIN SOP**

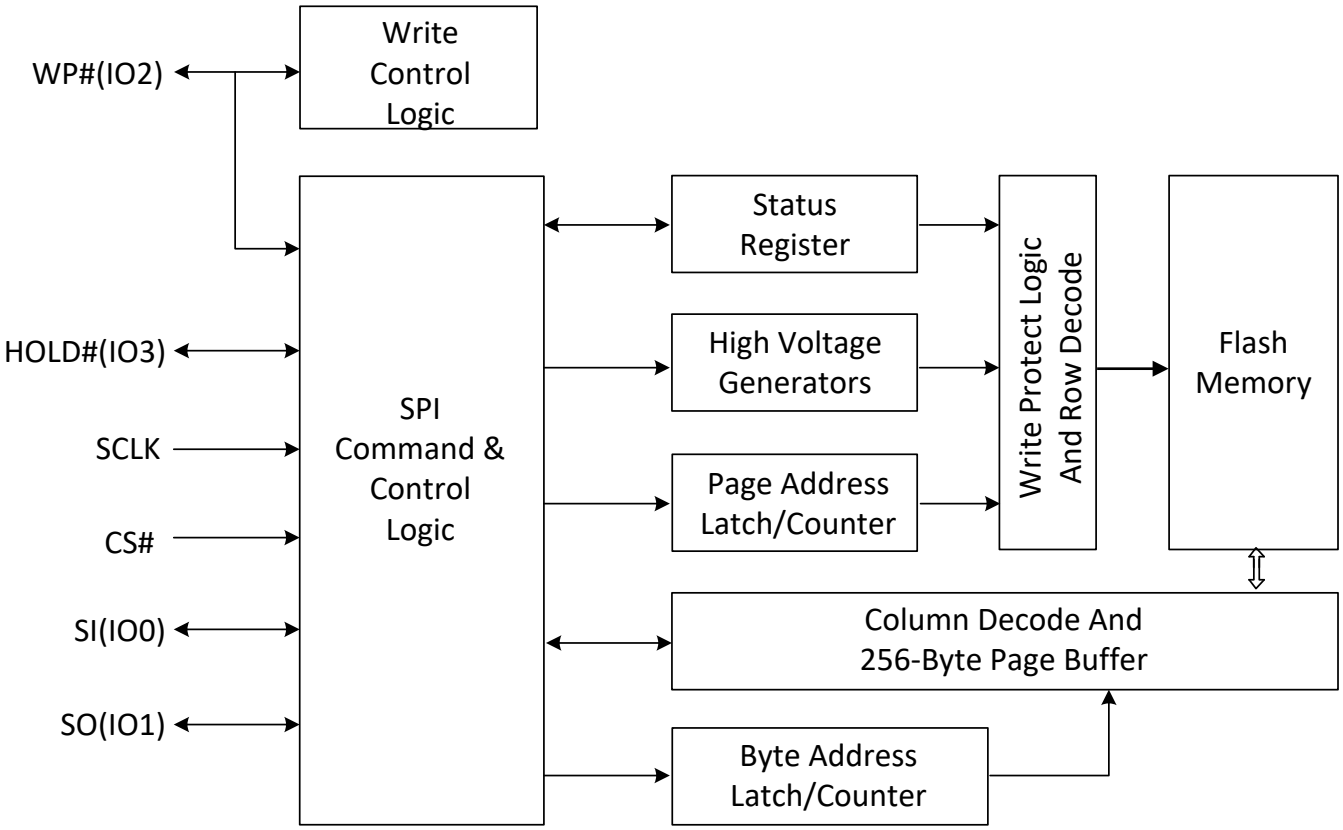



**8-PIN DFN/WSON**

## 1.3. Pin Description

| Pin Name | I/O | Description |
|---|---|---|
| **CS#** | I | Chip Select Input |
| **SO (IO1)** | I/O | Data Output (Data Input Output 1) |
| **WP# (IO2)** | I/O | Write Protect Input (Data Input Output 2) |
| **VSS** | | Ground |
| **SI (IO0)** | I/O | Data Input (Data Input Output 0) |
| **SCLK** | I | Serial Clock Input |
| **HOLD# (IO3)** | I/O | Hold Input (Data Input Output 3) |
| **VCC** | | Power Supply |

## 1.4. Block Diagram



# 2. MEMORY ORGANIZATION

## XT25F32F

| Each Device has | Each block has | Each sector has | Each page has | Remark |
|---|---|---|---|---|
| 4M | 64K/32K | 4K | 256 | bytes |
| 16K | 256/128 | 16 | - | pages |
| 1K | 16/8 | - | - | sectors |
| 64/128 | - | - | - | blocks |

## XT25F32F Block / Sector Architecture

| Block(64K-byte) | Block(32K-byte) | Sector | Address range | |
|---|---|---|---|---|
| 63 | 127 | 1023 | 3FF000H | 3FFFFFH |
| | | …… | …… | …… |
| | | 1016 | 3F8000H | 3F8FFFH |
| | 126 | 1015 | 3F7000H | 3F7FFFH |
| | | …… | …… | …… |
| | | 1008 | 3F0000H | 3F0FFFH |
| …… | …… | …… | …… | …… |
| | | …… | …… | …… |
| | | …… | …… | …… |
| | …… | …… | …… | …… |
| | | …… | …… | …… |
| | | …… | …… | …… |
| 1 | 3 | 31 | 01F000H | 01FFFFH |
| | | …… | …… | …… |
| | | 24 | 018000H | 018FFFH |
| | 2 | 23 | 017000H | 017FFFH |
| | | …… | …… | …… |
| | | 16 | 010000H | 010FFFH |
| 0 | 1 | 15 | 00F000H | 00FFFFH |
| | | …… | …… | …… |
| | | 8 | 008000H | 008FFFH |
| | 0 | 7 | 007000H | 007FFFH |
| | | …… | …… | …… |
| | | 0 | 000000H | 000FFFH |

# 3. DEVICE OPERATION

**Standard SPI**

The device features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

**Dual SPI**

The device supports Dual SPI operation when using the "Dual Output Fast Read" and "Dual I/O Fast Read" (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

**Quad SPI**

The device supports Quad SPI operation when using the "Quad Output Fast Read"," Quad I/O Fast Read"(6BH, EBH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

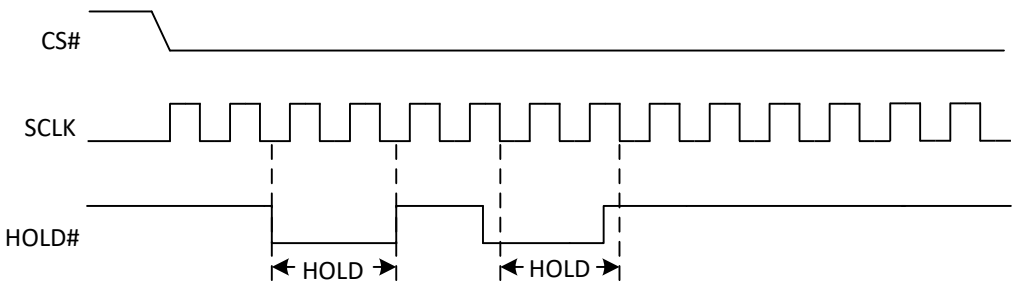
**Hold**

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during the HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

**Figure1. Hold Condition**



## The Reset Signaling Protocol (JEDEC 252)

The protocol consists of two phases: reset request, and completion (a device internal reset).

### Reset Request

1. CS# is driven active low to select the SPI slave (Note1)
2. Clock (SCK) remains stable in either a high or low state (Note 2)
3. SI / IO0 is driven low by the bus master, simultaneously with CS# going active low, (Note 3)
4. CS# is driven inactive (Note 4).

Repeat the steps 1-4 each time alternating the state of SI (Note 5).

NOTE 1 This powers up the SPI slave.

NOTE 2 This prevents any confusion with a command, as no command bits are transferred (clocked).

NOTE 3 No SPI bus slave drives SI during the CS# low before a transition of SCK, i.e., slave streaming output active is not allowed until after the first edge of SCK.

NOTE 4 The slave captures the state of SI on the rising edge of CS#.

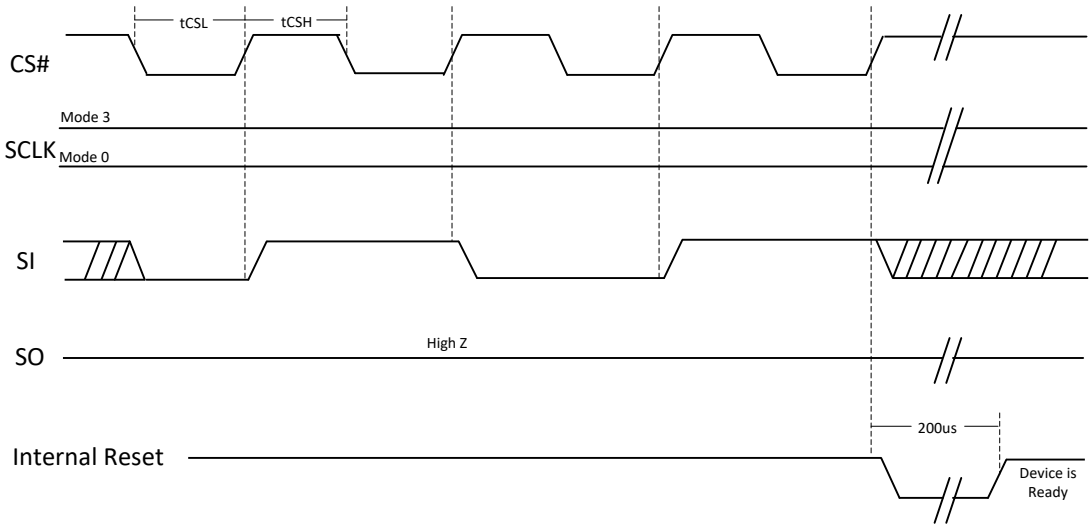
NOTE 5 SI is low on the first CS#, high on the second, low on the third, high on the fourth (This provides a 5h pattern, to differentiate it from random noise).

### Reset Completion

After the fourth CS# pulse, the slave triggers its internal reset.

### Timing Diagram and Timing Parameters

**Reset Signaling Protocol**



# 4. DATA PROTECTION

The XT25F32F provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up / Software Reset (66H + 99H)
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
  - Erase Security Register / Program Security Register
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits and CMP bit define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# goes low to prevent writing status register.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command (ABH) and software reset (66H+99H).

**Table 1.0 XT25F32F Protected area size (CMP=0)**

| Status Register Content | | | | | Memory Content | | | |
|---|---|---|---|---|---|---|---|---|
| BP4 | BP3 | BP2 | BP1 | BP0 | Blocks | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 63 | 3F0000H-3FFFFFH | 64KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 62 to 63 | 3E0000H-3FFFFFH | 128KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 60 to 63 | 3C0000H-3FFFFFH | 256KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 56 to 63 | 380000H-3FFFFFH | 512KB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 48 to 63 | 300000H-3FFFFFH | 1MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 32 to 63 | 200000H-3FFFFFH | 2MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 | 000000H-00FFFFH | 64KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 to 1 | 000000H-01FFFFH | 128KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 to 3 | 000000H-03FFFFH | 256KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 to 7 | 000000H-07FFFFH | 512KB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 to 15 | 000000H-0FFFFFH | 1MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 to 31 | 000000H-1FFFFFH | 2MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 to 63 | 000000H-3FFFFFH | 4MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 63 | 3FF000H-3FFFFFH | 4KB | Top Block |
| 1 | 0 | 0 | 1 | 0 | 63 | 3FE000H-3FFFFFH | 8KB | Top Block |
| 1 | 0 | 0 | 1 | 1 | 63 | 3FC000H-3FFFFFH | 16KB | Top Block |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | X | 63 | 3F8000H-3FFFFFH | 32KB | Top Block |
| 1 | 0 | 1 | 1 | 0 | 63 | 3F8000H-3FFFFFH | 32KB | Top Block |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000H-000FFFH | 4KB | Bottom Block |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000H-001FFFH | 8KB | Bottom Block |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000H-003FFFH | 16KB | Bottom Block |
| 1 | 1 | 1 | 0 | X | 0 | 000000H-007FFFH | 32KB | Bottom Block |
| 1 | 1 | 1 | 1 | 0 | 0 | 000000H-007FFFH | 32KB | Bottom Block |

**Table 1.1 XT25F32F Protected area size (CMP=1)**

| Status Register Content | | | | | Memory Content | | | |
|---|---|---|---|---|---|---|---|---|
| **BP4** | **BP3** | **BP2** | **BP1** | **BP0** | **Blocks** | **Addresses** | **Density** | **Portion** |
| X | X | 0 | 0 | 0 | ALL | 000000H-3FFFFFH | 4MB | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 to 62 | 000000H-3EFFFFH | 4032KB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 0 to 61 | 000000H-3DFFFFH | 3968KB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 0 to 59 | 000000H-3BFFFFH | 3840KB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 0 to 55 | 000000H-37FFFFH | 3584KB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 0 to 47 | 000000H-2FFFFFH | 3MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 0 to 31 | 000000H-1FFFFFH | 2MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 1 to 63 | 010000H-3FFFFFH | 4032KB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 2 to 63 | 020000H-3FFFFFH | 3968KB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 4 to 63 | 040000H-3FFFFFH | 3840KB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 8 to 63 | 080000H-3FFFFFH | 3584KB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 16 to 63 | 100000H-3FFFFFH | 3MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 32 to 63 | 200000H-3FFFFFH | 2MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 to 63 | 000000H-3FEFFFH | 4092KB | L-1023/1024 |
| 1 | 0 | 0 | 1 | 0 | 0 to 63 | 000000H-3FDFFFH | 4088KB | L-511/512 |
| 1 | 0 | 0 | 1 | 1 | 0 to 63 | 000000H-3FBFFFH | 4080KB | L-255/256 |
| 1 | 0 | 1 | 0 | X | 0 to 63 | 000000H-3F7FFFH | 4064KB | L-127/128 |
| 1 | 0 | 1 | 1 | 0 | 0 to 63 | 000000H-3F7FFFH | 4064KB | L-127/128 |
| 1 | 1 | 0 | 0 | 1 | 0 to 63 | 001000H-3FFFFFH | 4092KB | U-1023/1024 |
| 1 | 1 | 0 | 1 | 0 | 0 to 63 | 002000H-3FFFFFH | 4088KB | U-511/512 |
| 1 | 1 | 0 | 1 | 1 | 0 to 63 | 004000H-3FFFFFH | 4080KB | U-255/256 |
| 1 | 1 | 1 | 0 | X | 0 to 63 | 008000H-3FFFFFH | 4064KB | U-127/128 |
| 1 | 1 | 1 | 1 | 0 | 0 to 63 | 008000H-3FFFFFH | 4064KB | U-127/128 |

# 5. STATUS REGISTER

Table2.1 Status Register-1

| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
|---|---|---|---|---|---|---|---|
| SRP0 | BP4 | BP3 | BP2 | BP1 | BP0 | WEL | WIP |
| Status Register Protection Bit | Block Protect Bit | Block Protect Bit | Block Protect Bit | Block Protect Bit | Block Protect Bit | Write Enable Latch | Erase/Write In Progress |
| Non-volatile | Non-volatile | Non-volatile | Non-volatile | Non-volatile | Non-volatile | Volatile, Read Only | Volatile, Read Only |

Table2.2 Status Register-2

| S15 | S14 | S13 | S12 | S11 | S10 | S9 | S8 |
|---|---|---|---|---|---|---|---|
| Reserved | CMP | LB3 | LB2 | LB1 | Reserved | QE | SRP1 |
| Reserved | Complement Protect Bit | Security Register Lock Bit | Security Register Lock Bit | Security Register Lock Bit | Reserved | Quad Enable | Status Register Protection Bit |
| Reserved | Non-volatile | Non-volatile writable (OTP) | Non-volatile writable (OTP) | Non-volatile writable (OTP) | Reserved | Non-volatile | Non-volatile |

Table2.3 Status Register-3

| S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 |
|---|---|---|---|---|---|---|---|
| Reserved | DRV1 | DRV0 | Reserved | Reserved | Reserved | Reserved | DC |
| Reserved | Output Driver Strength | Output Driver Strength | Reserved | Reserved | Reserved | Reserved | Dummy Configuration Bit |
| Reserved | Non-volatile | Non-volatile | Reserved | Reserved | Reserved | Reserved | Non-volatile |

The status and control bits of the Status Register are as follows:

### WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

### WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

### BP4,BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 1.0 & 1.1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

### SRP1, SRP0

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the type of write protection: software protection, hardware protection, power supply lock-down or one-time programmable protection.

| SRP1 | SRP0 | WP# | Status Register | Description |
|---|---|---|---|---|
| 0 | 0 | X | Software Protected | The Status Register can be written to after a Write Enable command, WEL=1. (Default) |
| 0 | 1 | 0 | Hardware Protected | WP#=0, the Status Register locked and cannot be written to. |
| 0 | 1 | 1 | Hardware Unprotected | WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1. |
| 1 | 0 | X | Power Supply Lock-Down | Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle. [Note 1] |
| 1 | 1 | X | One-Time Program [Note 2] | Status Register is protected and cannot be written to. |

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact XTX for details.

### QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground).

### LB3, LB2, LB1 bit.

The LB3, LB2,LB1 bit are non-volatile One Time Program (OTP) bits in Status Register (S13,S12,S11) that provide the write protect control and status to the Security Registers. The default state of LB3, LB2, LB1 bits are 0, the corresponding security registers are unlocked. LB3,LB2,LB1 can be set to 1 using the Write Register instruction. LB3, LB2, LB1 are One Time Programmable, once they are set to 1, the corresponding Security Register will become read-only permanently.

### CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

### DC bit

The Dummy Configuration (DC) bit is non-volatile, which selects the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured.

| Command | DC Bit | Dummy clock cycles | Freq. |
|---|---|---|---|
| BBH | 0 (Default) | 4 | 104Mhz |
| | 1 | 8 | 133Mhz |
| EBH | 0 (Default) | 6 | 104Mhz |
| | 1 | 10 | 133Mhz |

### DRV1, DRV0

The Output Driver Strength (DRV1 & DRV0) bits are used to determine the output driver strength for the Read operations.

Table 2.4 DRV1, DRV0 Driver Strength Table

| DRV1 | DRV0 | Driver Strength |
|---|---|---|
| 0 | 0 | 25% |
| 0 | 1 | 50% |
| 1 | 0 | 75% (default) |
| 1 | 1 | 100% |

# 6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 3, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

**Table 3. Commands**

| Command Name | Byte1 | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 | n-Bytes |
|---|---|---|---|---|---|---|---|
| Write Enable | 06H | | | | | | |
| Write Enable for Volatile Status Register | 50H | | | | | | |
| Write Disable | 04H | | | | | | |
| Read Status Register-1 | 05H | (S7-S0) | | | | | (continuous) |
| Read Status Register-2 | 35H | (S15-S8) | | | | | (continuous) |
| Read Status Register-3 | 15H | (S23-S16) | | | | | (continuous) |
| Write Status Register-1 | 01H | (S7-S0) | (S15-S8) | | | | |
| Write Status Register-2 | 31H | (S15-S8) | | | | | |
| Write Status Register-3 | 11H | (S23-S16) | | | | | |
| Read Data | 03H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | | (continuous) |
| Fast Read | 0BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (continuous) |
| Dual Output Fast Read | 3BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(1) | (continuous) |
| Dual I/O Fast Read | BBH | A23-A8(2) | A7-A0 M7-M0(2) | (D7-D0)(1) | | | (continuous) |
| Quad Output Fast Read | 6BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(3) | (continuous) |
| Quad I/O Fast Read | EBH | A23-A0 M7-M0(4) | Dummy(5) | (D7-D0)(3) | | | (continuous) |
| Page Program | 02H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | | (to byte256) |
| Quad Page Program | 32H | A23-A16 | A15-A8 | A7-A0 | (D7-D0)(3) | | (to byte256) |
| Sector Erase | 20H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(32KB) | 52H | A23-A16 | A15-A8 | A7-A0 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Block Erase(64KB) | D8H | A23-A16 | A15-A8 | A7-A0 | | | |
| Chip Erase | C7/60H | | | | | | |
| Set Burst with Wrap | 77H | dummy | dummy | dummy | W6-W4 | | |
| Deep Power-Down | B9H | | | | | | |
| Release From Deep Power-Down, And Read Device ID | ABH | dummy | dummy | dummy | (DID7-DID0) | | (continuous) |
| Release From Deep Power-Down | ABH | | | | | | |
| Manufacturer/Device ID | 90H | A23-A16 | A15-A8 | A7-A0 | (MID7-MID0) | (DID7-DID0) | (continuous) |
| Read Serial Flash Discoverable Parameters | 5AH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (continuous) |
| Read Unique ID | 4BH | dummy | dummy | dummy | dummy | (UID127-UID120) | (to UID0) |
| Read Identification | 9FH | (MID7-MID0) | (JDID15-JDID8) | (JDID7-JDID0) | | | (continuous) |
| Erase Security Register(6) | 44H | A23-A16 | A15-A8 | A7-A0 | | | |
| Program Security Register(6) | 42H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | (Next byte) | (to byte256) |
| Read Security Register(6) | 48H | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (to byte256) |
| Enable Reset | 66H | | | | | | |
| Reset | 99H | | | | | | |

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8,A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9,A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

   IO0 = (D4, D0, .....)

   IO1 = (D5, D1, .....)

   IO2 = (D6, D2, .....)

   IO3 = (D7, D3, .....)

4. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Quad I/O Fast Read Data

IO0 = (x, x, x, x, D4, D0,…)

IO1 = (x, x, x, x, D5, D1,…)

IO2 = (x, x, x, x, D6, D2,…)

IO3 = (x, x, x, x, D7, D3,…)

6. Security Registers Address:

Security Register1: A23-A16=00H, A15-A8=10H, A7-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A8=20H, A7-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A8=30H, A7-A0= Byte Address.

## Table of ID Definitions:

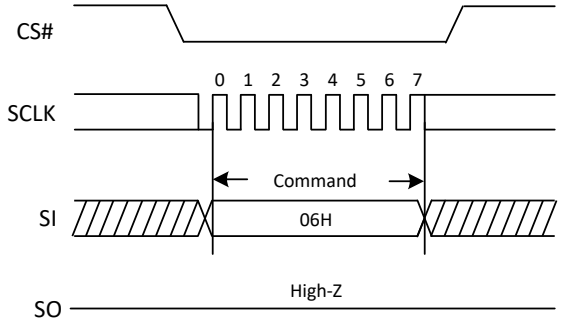
XT25F32F

| Operation Code | MID7-MID0 | ID15-ID8 | ID7-ID0 |
|---|---|---|---|
| 9FH | 0B | 40 | 16 |
| 90H | 0B | | 15 |
| ABH | | | 15 |

## 6.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Erase/Program Security Register and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low → Sending the Write Enable command →CS# goes high.

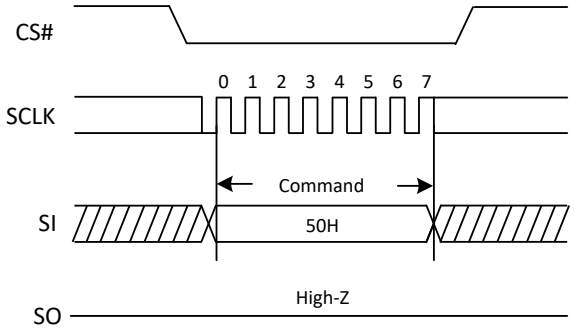
**Figure 2. Write Enable Sequence Diagram**




## 6.2. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

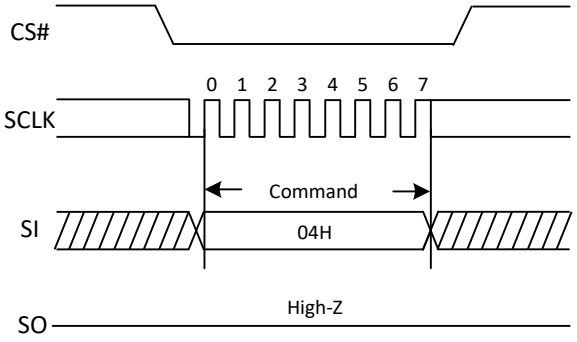
**Figure 3. Write Enable for Volatile Status Register Sequence Diagram**



## 6.3. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

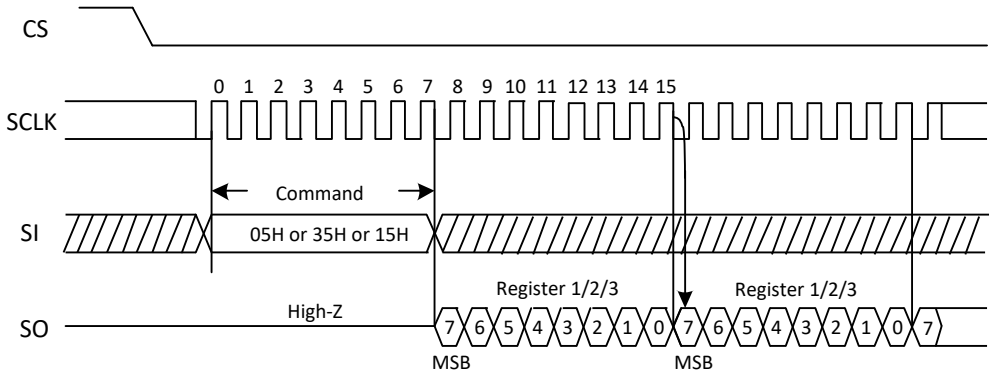
**Figure 4. Write Disable Sequence Diagram**




## 6.4. Read Status Register (RDSR) (05H or 35H or 15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H", the SO will output Status Register bits S7~S0. The command code "35H", the SO will output Status Register bits S15~S8. The command code "15H", the SO will output Status Register bits S23~S16.

**Figure 5. Read Status Register Sequence Diagram**



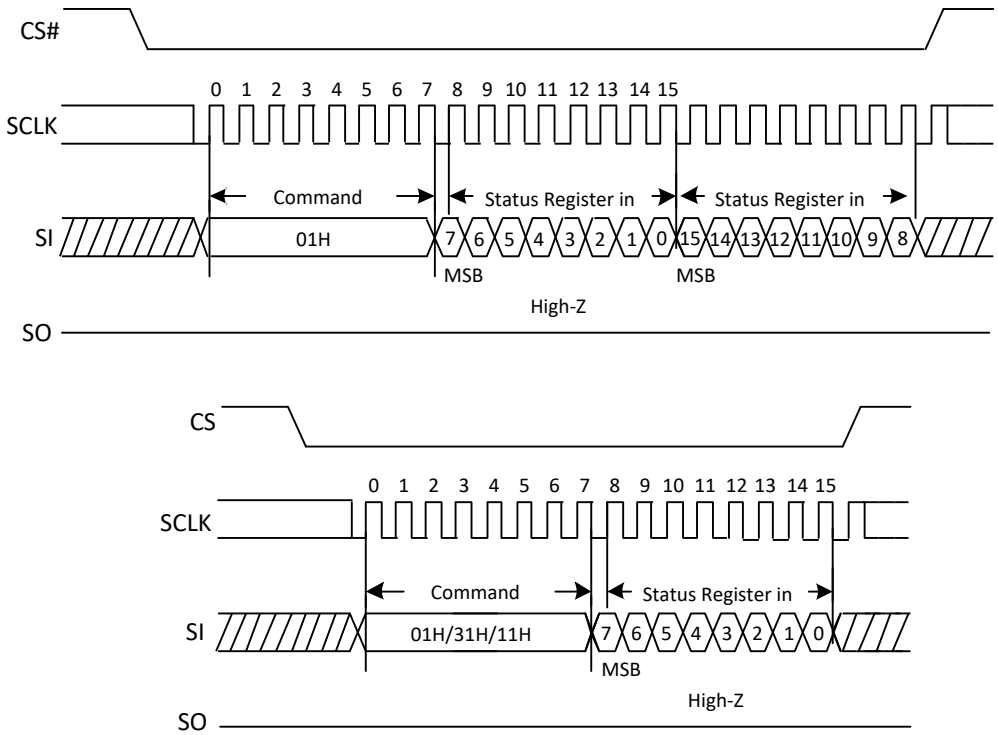
## 6.5. Write Status Register (WRSR) (01H or 31H or 11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on the volatile bits of the Status Register. CS# must be driven high after the eighth or sixteenth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1.0 & 1.1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered. For command code “01H”, the SI will input Status Register bits S7~S0, S15~S8. For the command code “31H”, the SI will input Status Register bits S15~S8. For the command code “11H”, the SI will input Status Register bits S23~S16.

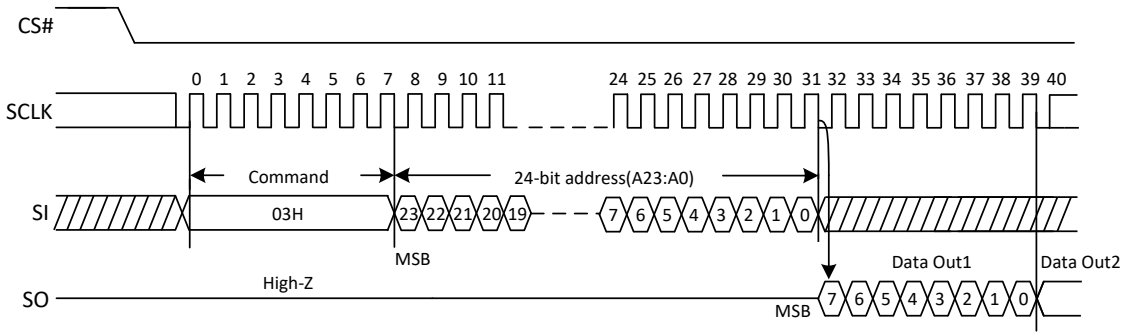
**Figure 6. Write Status Register Sequence Diagram**



## 6.6. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

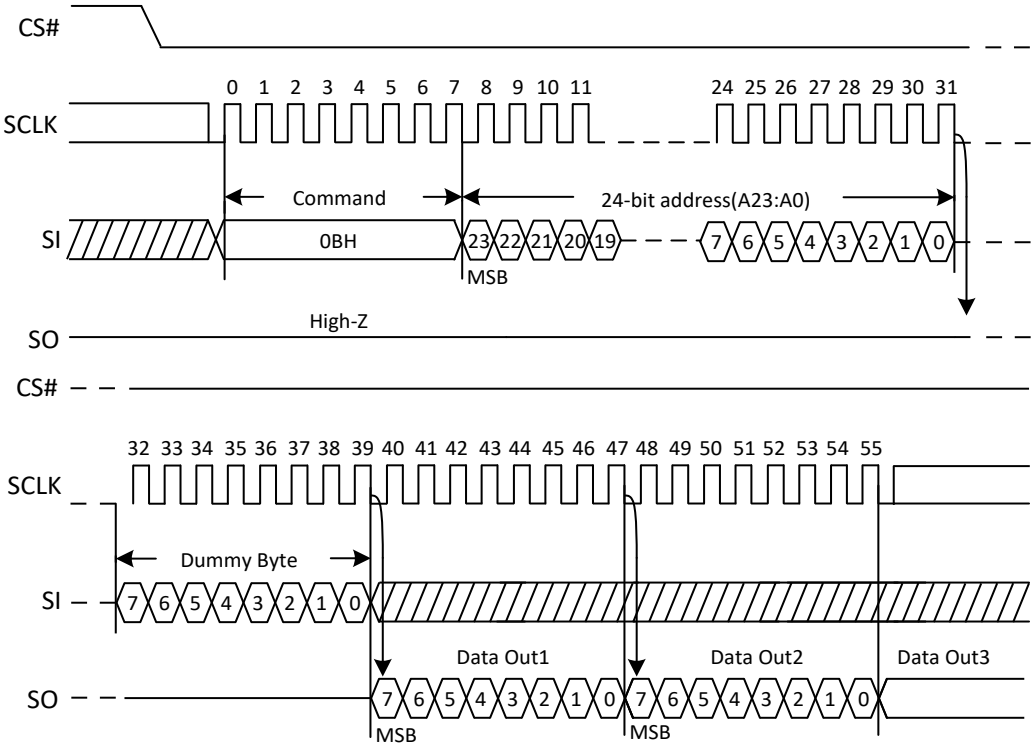
**Figure 7. Read Data Bytes Sequence Diagram**




## 6.7. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for fast reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

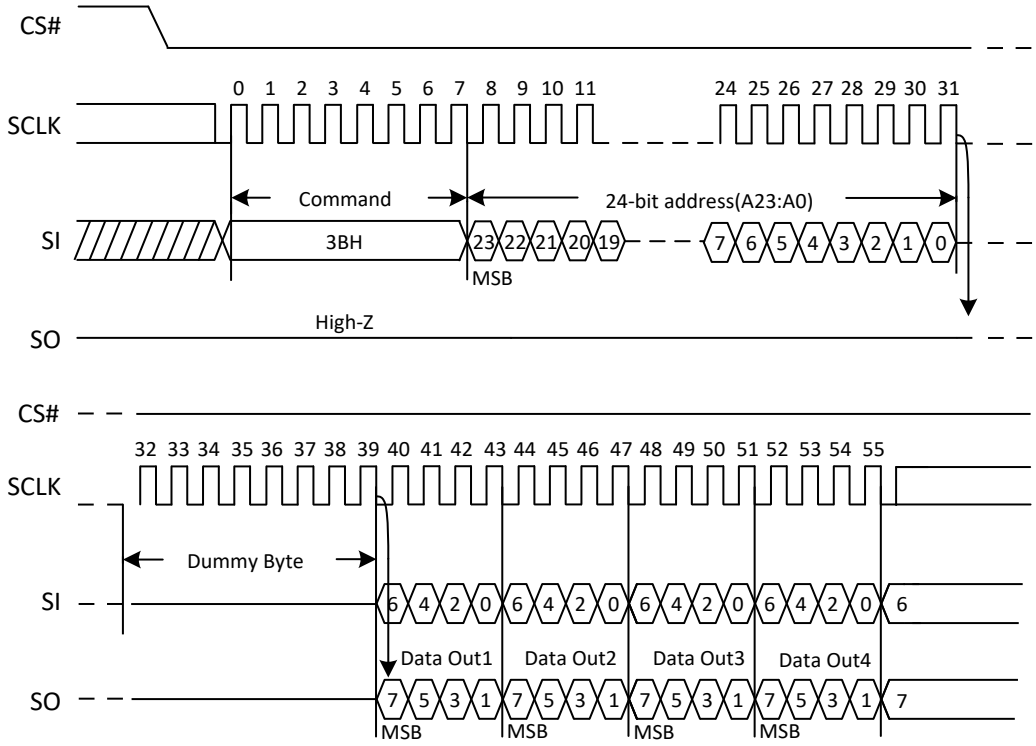
**Figure 8. Read Data Bytes at Higher Speed Sequence Diagram**



## 6.8. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

**Figure 9. Dual Output Fast Read Sequence Diagram**



## 6.10. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

The number of dummy clocks is 4 by default (M7-M0 Byte is considered to be 4 dummy clocks). Also can be set to 8 by the DC bit of Status Register.

**Dual I/O Fast Read with “Continuous Read Mode”**

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7- 0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5- 4) =(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure 10a. If the “Continuous Read Mode” bits (M5- 4) do not equal to (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

**Figure 10. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))**

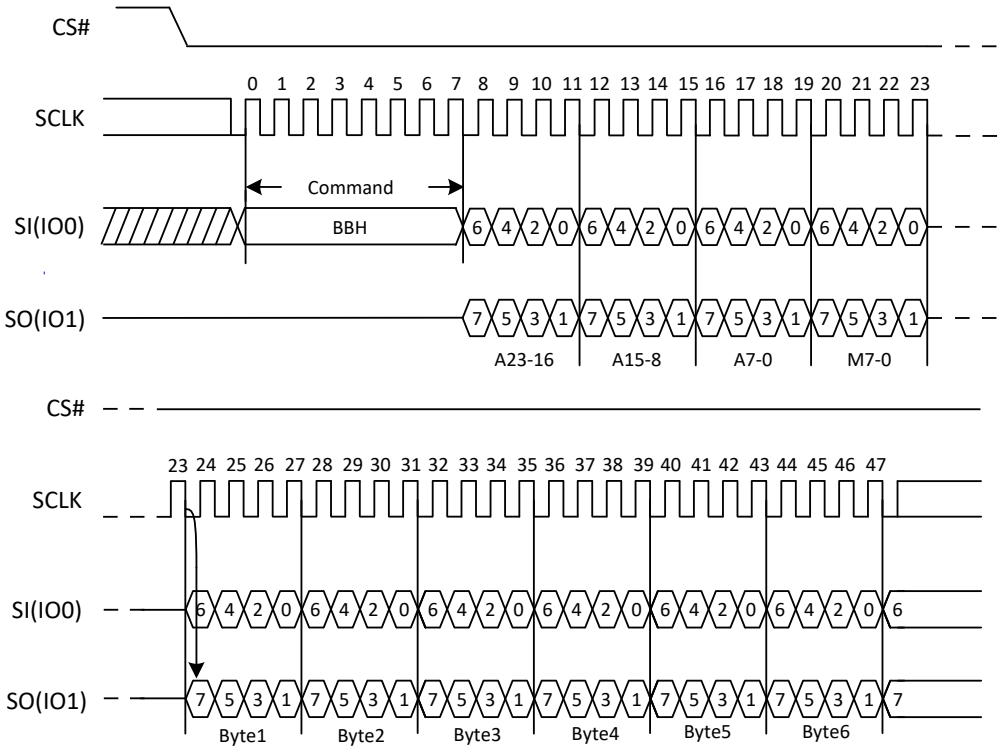
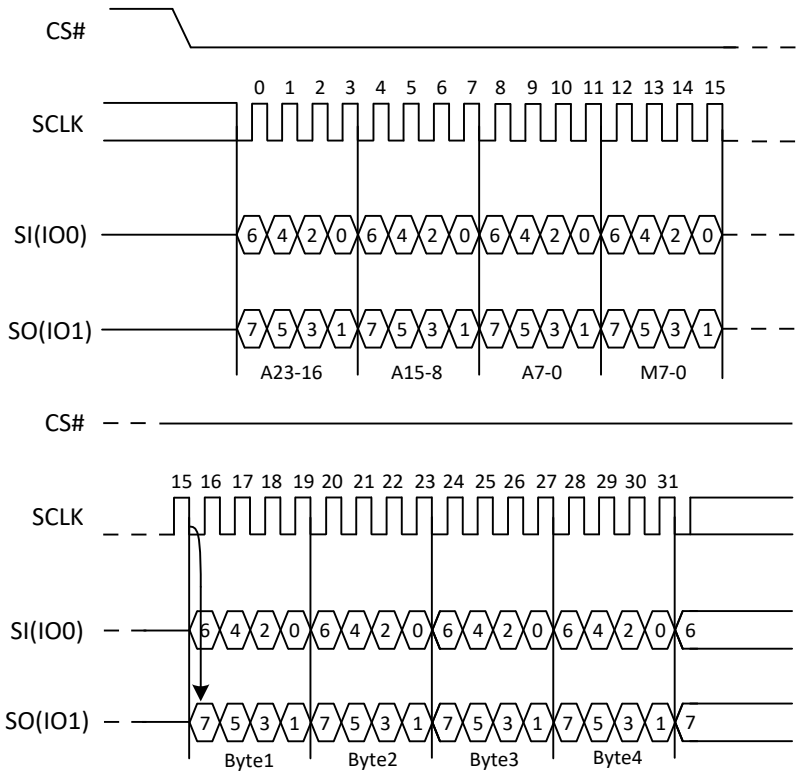


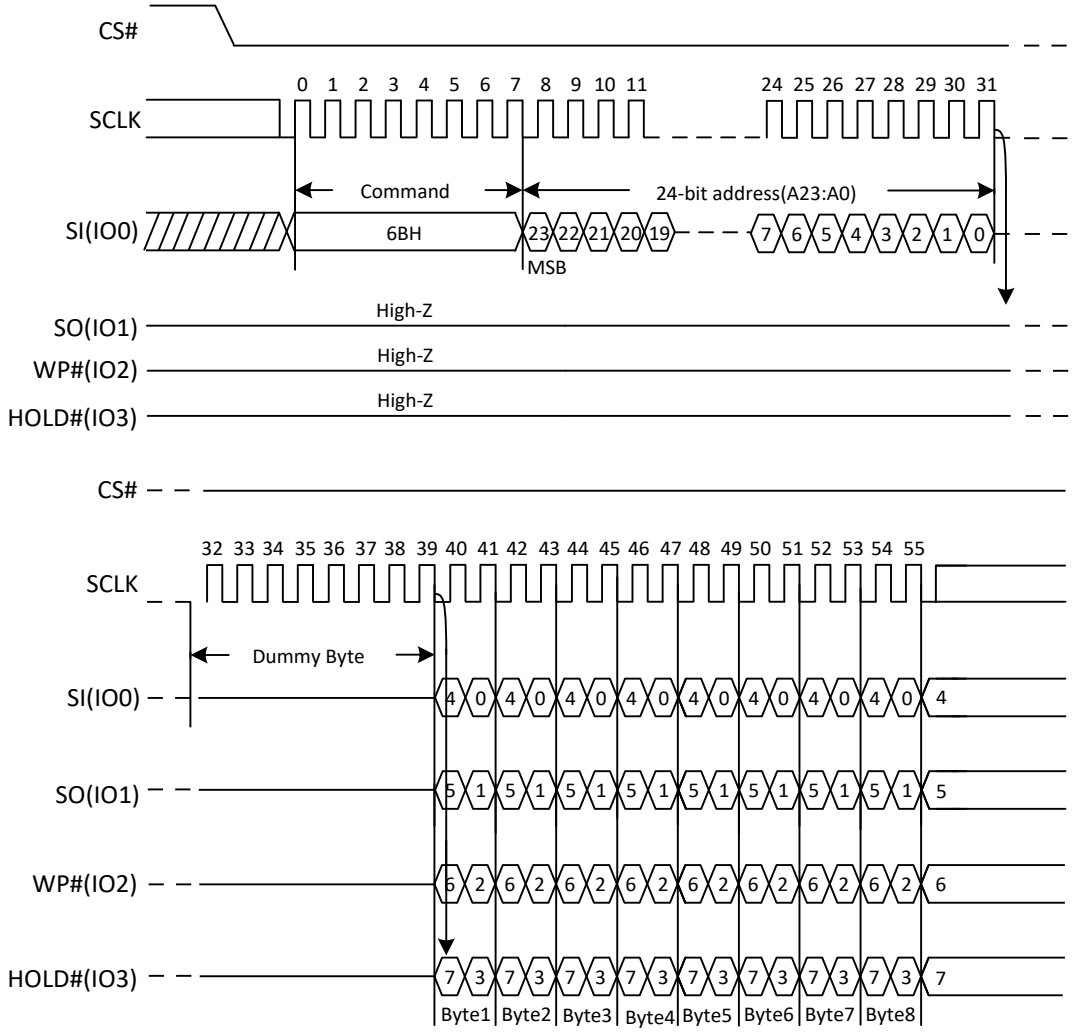
**Figure 10a. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))**



## 6.11. Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in Figure 11. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

**Figure 11. Quad Output Fast Read Sequence Diagram**

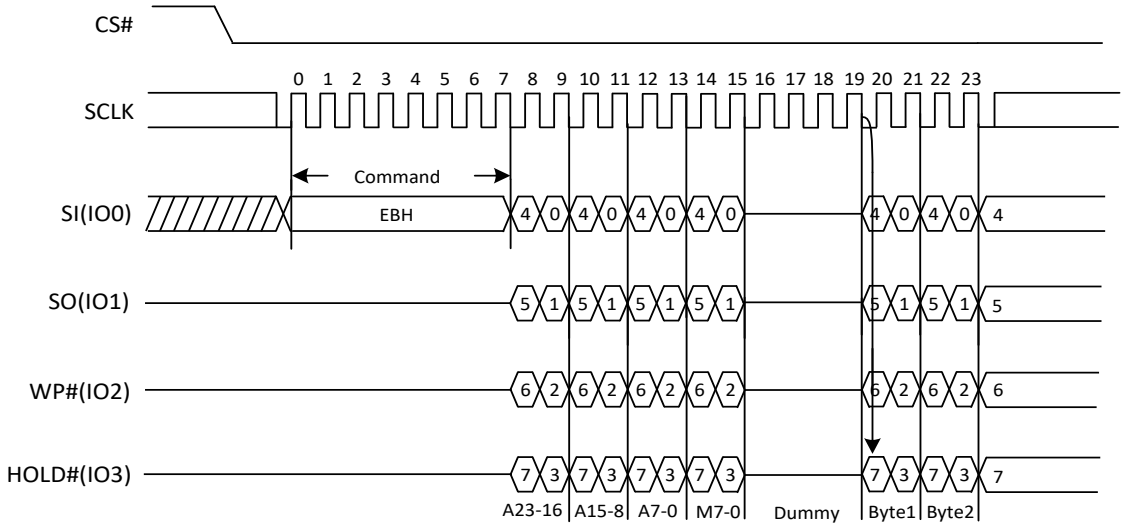



## 6.12. Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4 dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in Figure 12. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

The number of dummy clocks is 6 by default (M7-M0 Byte is considered to be 2 dummy clocks). Also can be set to 10 by the DC bit of Status Register.

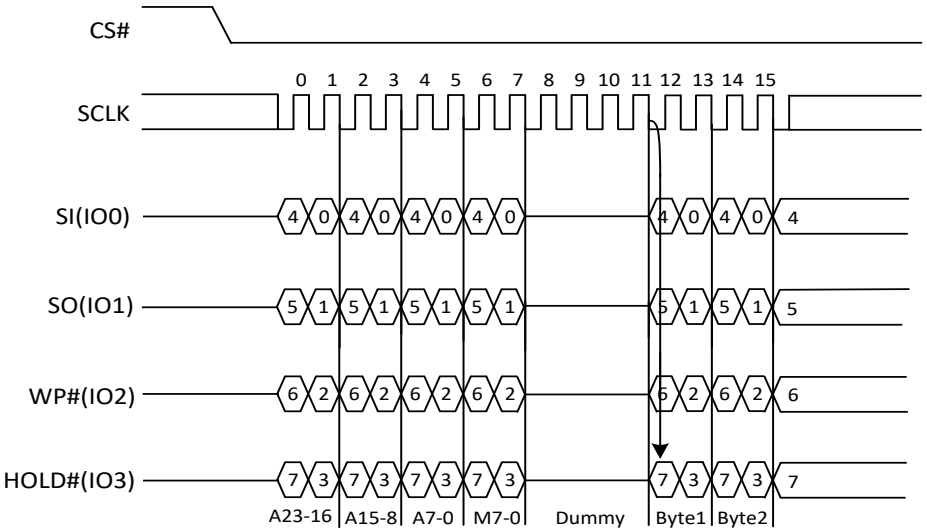
**Figure 12. Quad I/O Fast Read Sequence Diagram (M5-4≠(1, 0))**




## Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) =(1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in Figure 12a. If the "Continuous Read Mode" (M5- 4) do not equal to (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.

**Figure 12a. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0))**




## Quad I/O Fast Read with ""8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

## 6.13. Page Program (PP) (02H)

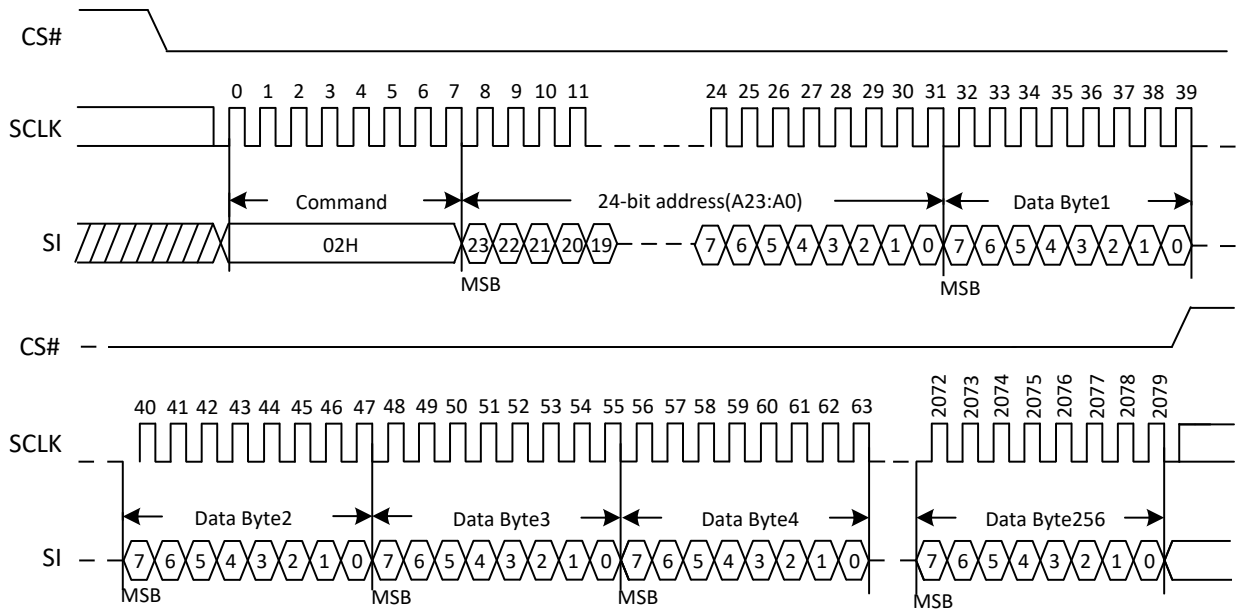
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low →Sending Page Program command →3-byte address on SI →at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure 13. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

**Figure 13. Page Program Sequence Diagram**



## 6.14. Quad Page Program (QPP) (32H)

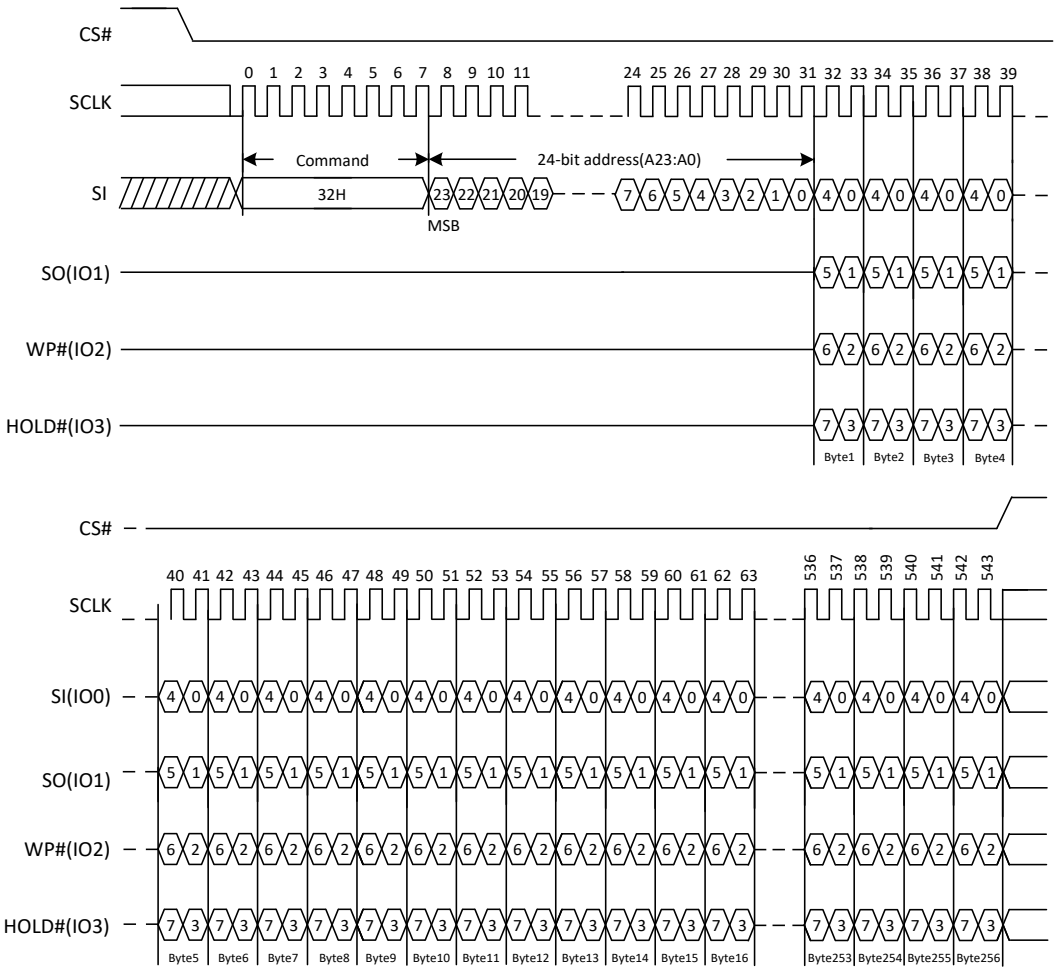
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit 9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure 14. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) will not be executed.

**Figure 14. Quad Page Program Sequence Diagram**

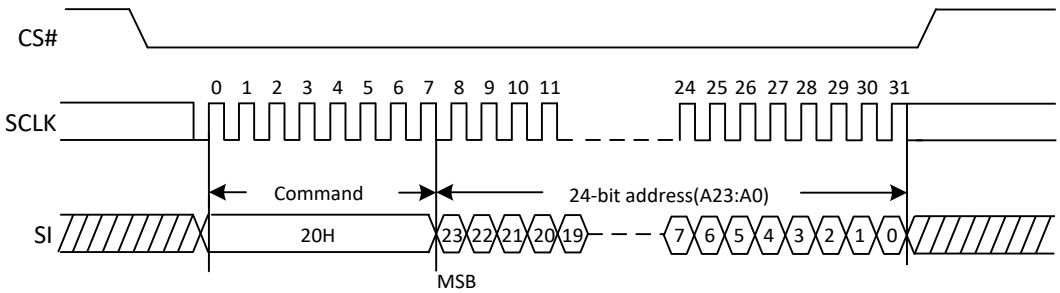


## 6.15. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → Sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 15. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) com-mand applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table 1.0 & 1.1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

**Figure 15. Sector Erase Sequence Diagram**

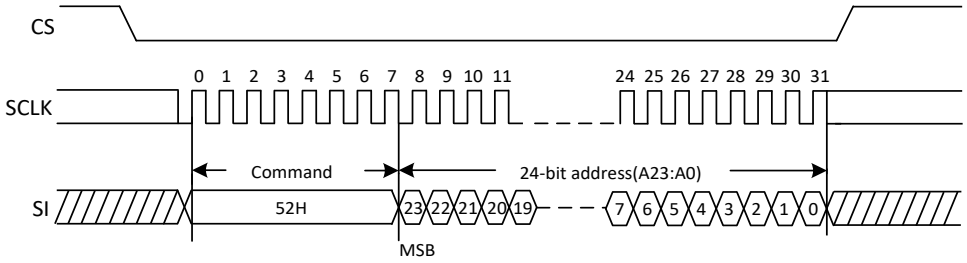



## 6.16. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low →Sending 32KB Block Erase command → 3-byte address on SI →CS# goes high. The command sequence is shown in Figure 16. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 1.0 & 1.1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

**Figure 16. 32KB Block Erase Sequence Diagram**

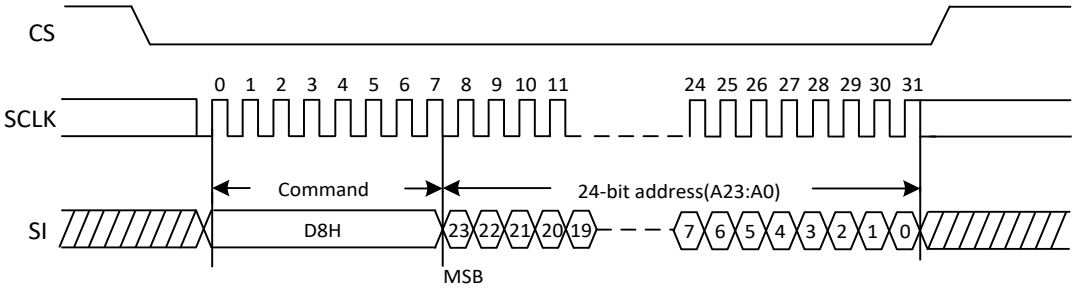



## 6.17. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → Sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 17. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 1.0 & 1.1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

**Figure 17. 64KB Block Erase Sequence Diagram**

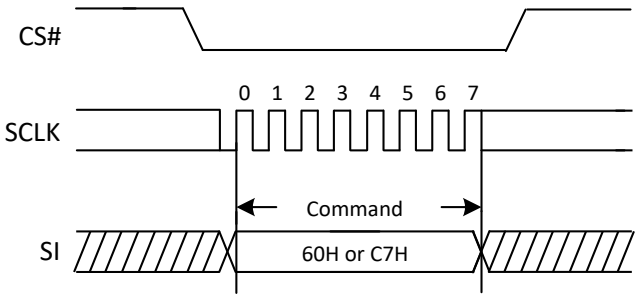


## 6.18. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low→Sending Chip Erase command→CS# goes high. The command sequence is shown in Figure 18. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is $t_{CE}$) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or the Block Protect (BP2,BP1,and BP0)bits are 1 and CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected. Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

**Figure 18. Chip Erase Sequence Diagram**



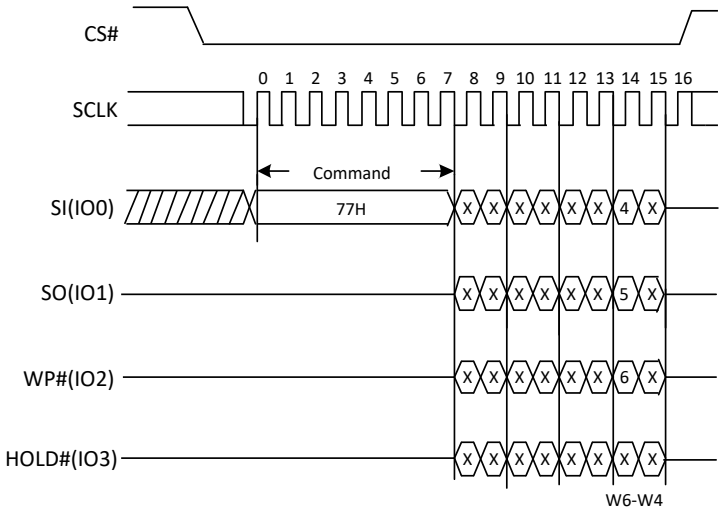
## 6.19. Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode. The Set Burst with Wrap command sequence: CS# goes low →Send Set Burst with Wrap command →Send 24 dummy bits →Send 8 bits "Wrap bits"→CS# goes high

| W6,W5 | W4=0 | | W4=1(default) | |
|---|---|---|---|---|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0,0 | Yes | 8-byte | No | N/A |
| 0,1 | Yes | 16-byte | No | N/A |
| 1,0 | Yes | 32-byte | No | N/A |
| 1,1 | Yes | 64-byte | No | N/A |

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

**Figure 19. Set Burst with Wrap Sequence Diagram**



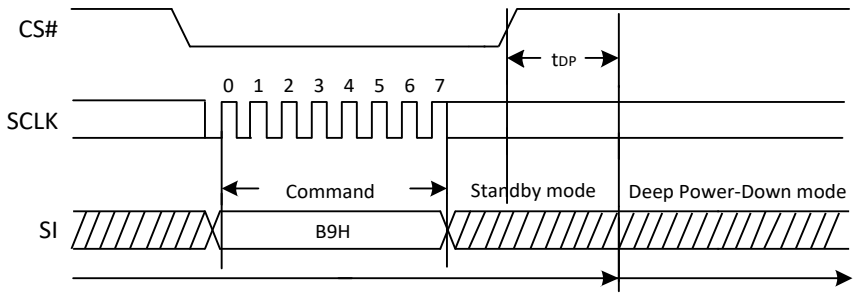
## 6.20. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID command (ABH) and software reset (66H+99H). This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command (ABH) also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low→Sending Deep Power-Down command→CS# goes high. The command sequence is shown in Figure 20. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 20. Deep Power-Down Sequence Diagram**



## 6.21. Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read/Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure 21. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3 dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 21a. The Device ID value for the XT25F16F is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 21a, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals to 1) the command is ignored and will not affect the current cycle.

**Figure 21. Release Power-Down Sequence Diagram**

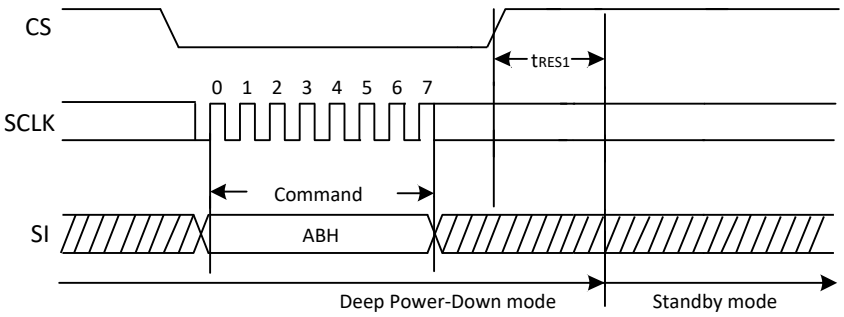
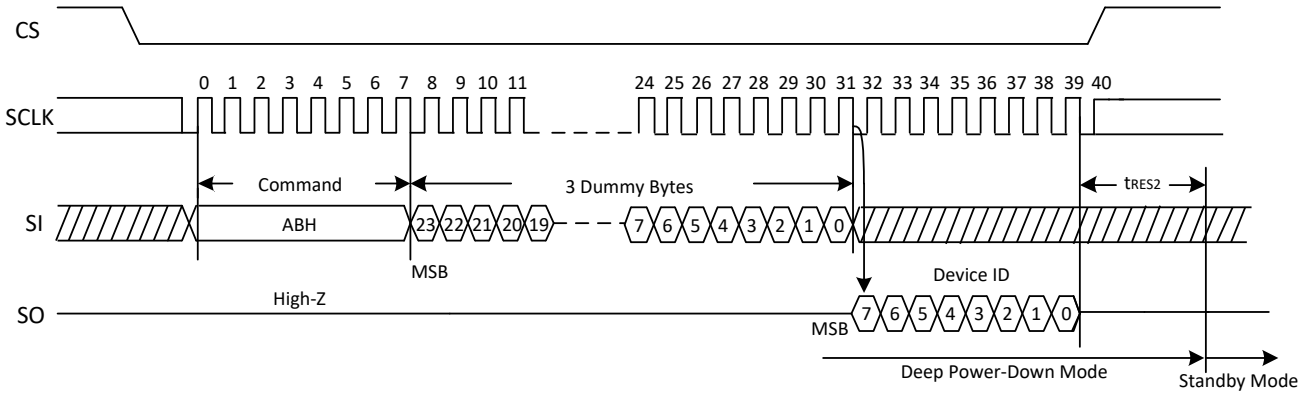



**Figure 21a. Release Power-Down/Read Device ID Sequence Diagram**

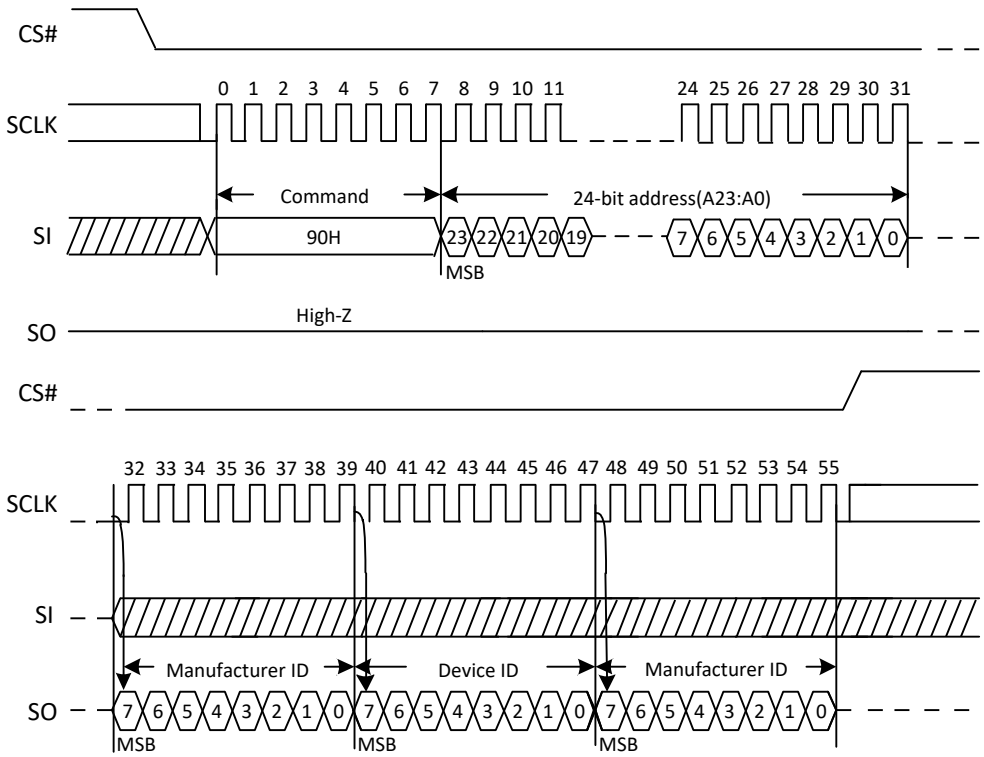


## 6.22. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in the figure below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

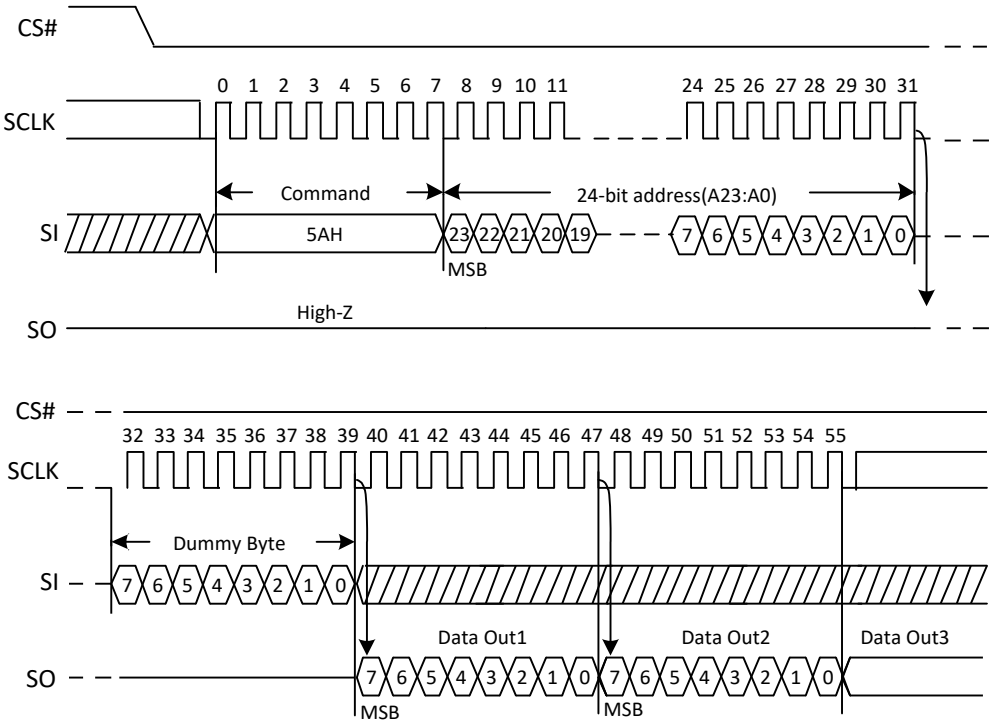
**Figure 22. Read Manufacture ID/ Device ID Sequence Diagram**




## 6.23. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

**Figure 23. Read Serial Flash Discoverable Parameter command Sequence Diagram**




Note: A23-A8 = 0, A7-A0 is the starting byte address for 256-byte SFDP Register.

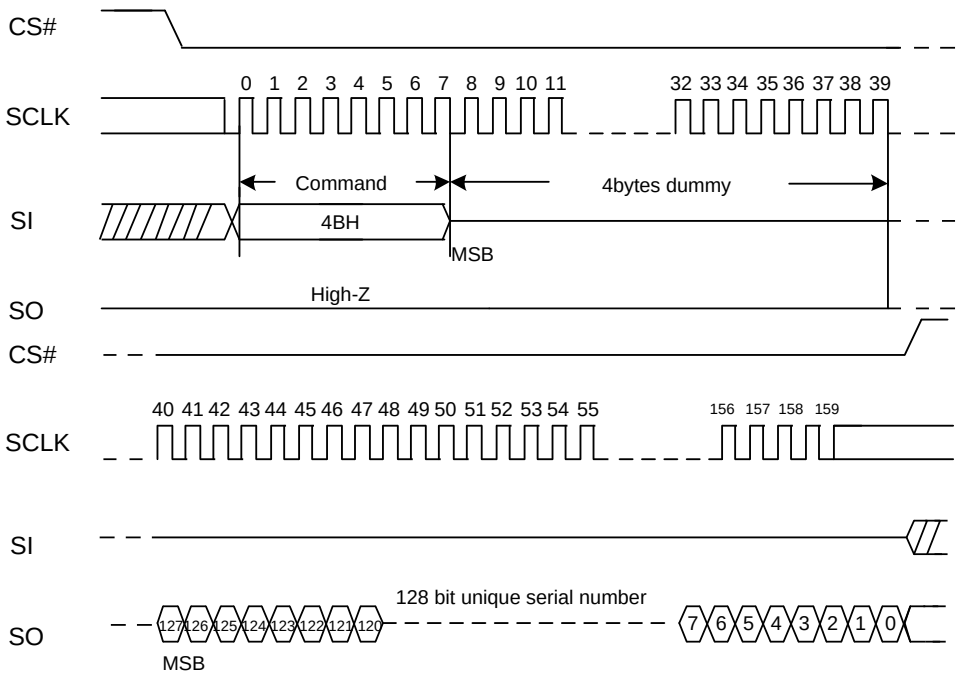
## 6.24. Read Unique ID(4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → Sending Read Unique ID command →4 dummy bytes→ 128bit Unique ID Out → CS# goes high.

The command sequence is show below.

**Figure 24. Read Unique ID (RUID) Sequence (Command 4BH)**

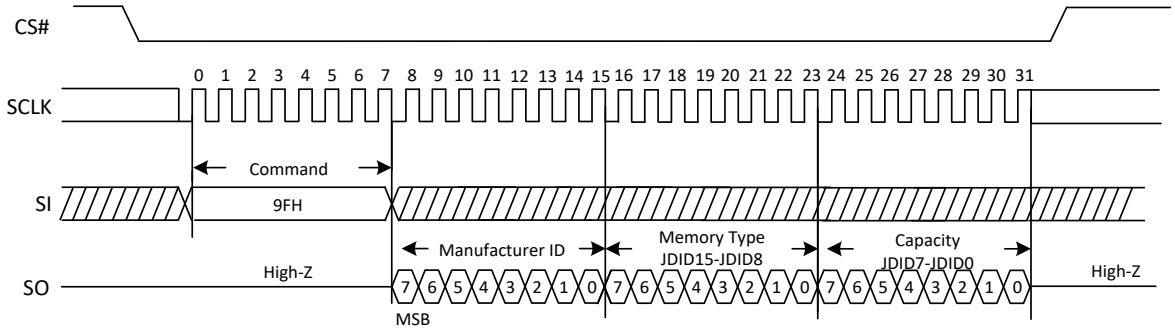



## 6.25. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure 25. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

**Figure 25. Read Identification ID Sequence Diagram**




## 6.26. Erase Security Registers (44H)

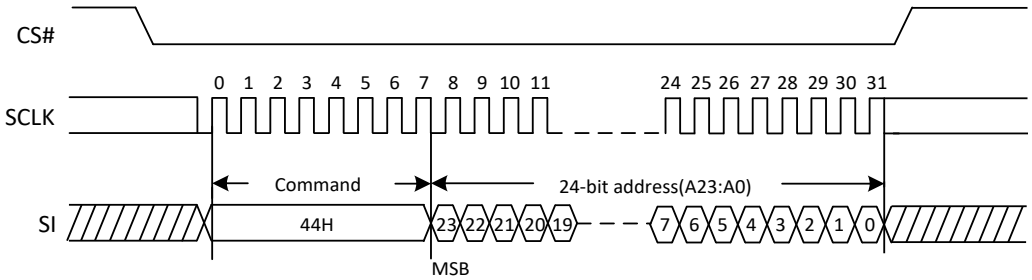
The device provides 3x1024-byte Security Registers which only erased each 1024-byte at once. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low→ Sending Erase Security Registers Command→CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB1,LB2,LB3) in the Status Register can be used to OTP protect the corresponding security registers (#1, #2, #3). Once the LB bit is set to 1, the corresponding Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

| Address | A23-A16 | A15-A12 | A11-A10 | A9-A0 |
|---|---|---|---|---|
| Security Registers #1 | 00000000 | 0001b | 00b | Don't Care |
| Security Registers #2 | 00000000 | 0010b | 00b | Don't Care |
| Security Registers #3 | 00000000 | 0011b | 00b | Don't Care |

**Figure 26. Erase Security Registers command Sequence Diagram**



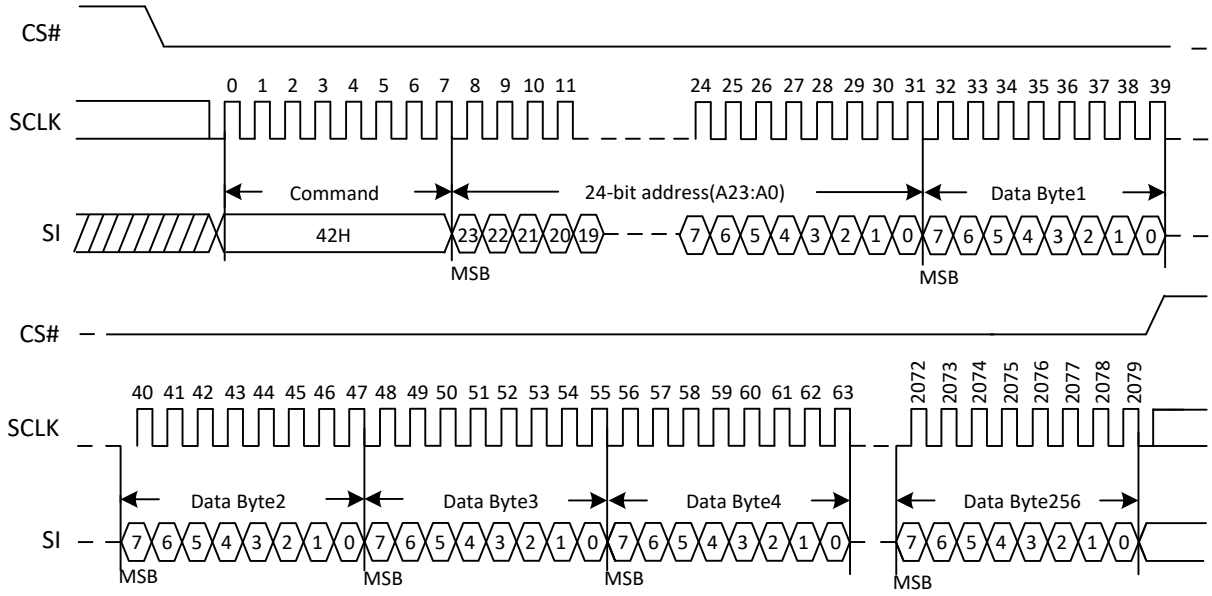
## 6.27. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB1,LB2,LB3) is set to 1, the corresponding Security Registers (#1, #2, #3) will be permanently locked. Program Security Registers command will be ignored.

| Address | A23-A16 | A15-A12 | A11-A10 | A9-A0 |
|---|---|---|---|---|
| Security Registers #1 | 00000000 | 0001b | 00b | Byte Address |
| Security Registers #2 | 00000000 | 0010b | 00b | Byte Address |
| Security Registers #3 | 00000000 | 0011b | 00b | Byte Address |

**Figure 27. Program Security Registers command Sequence Diagram**

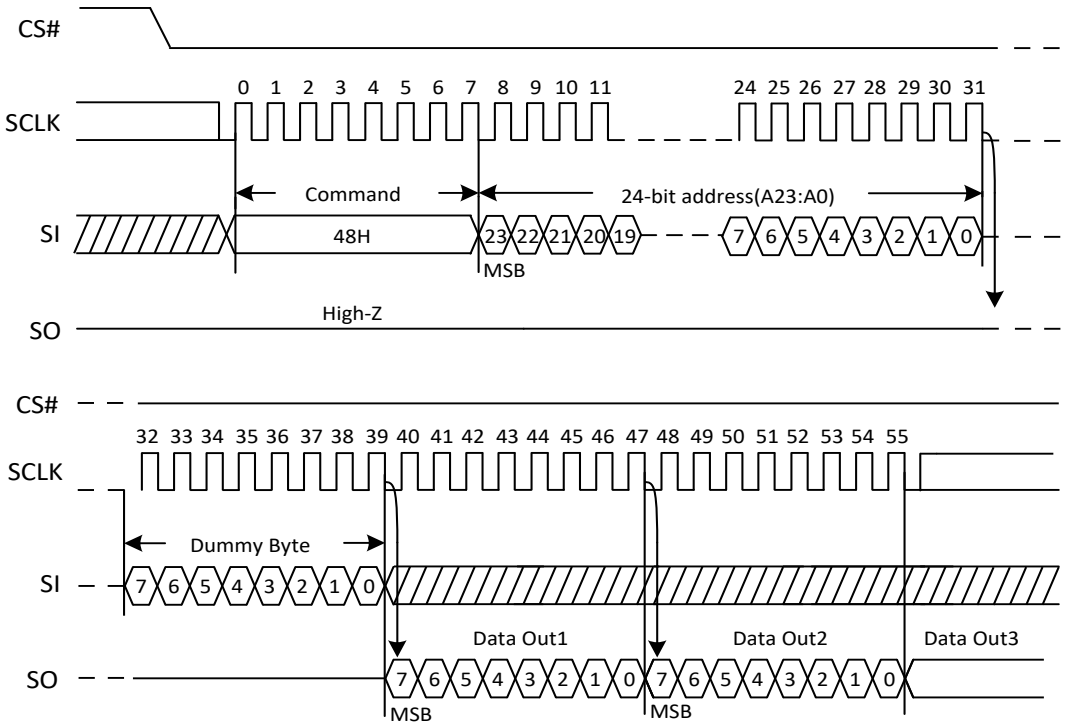


## 6.28. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

| Address | A23-A16 | A15-A12 | A11-A10 | A9-A0 |
|---|---|---|---|---|
| Security Registers #1 | 00000000 | 0001b | 00b | Byte Address |
| Security Registers #2 | 00000000 | 0010b | 00b | Byte Address |
| Security Registers #3 | 00000000 | 0011b | 00b | Byte Address |

**Figure 28. Read Security Registers command Sequence Diagram**



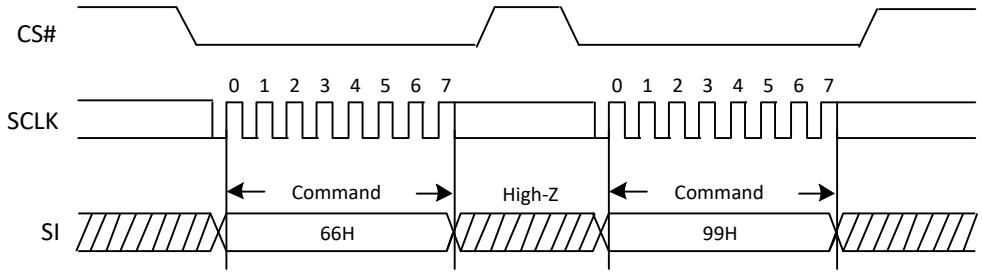
## 6.29. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Read Parameter setting (P7-P0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command sequence.

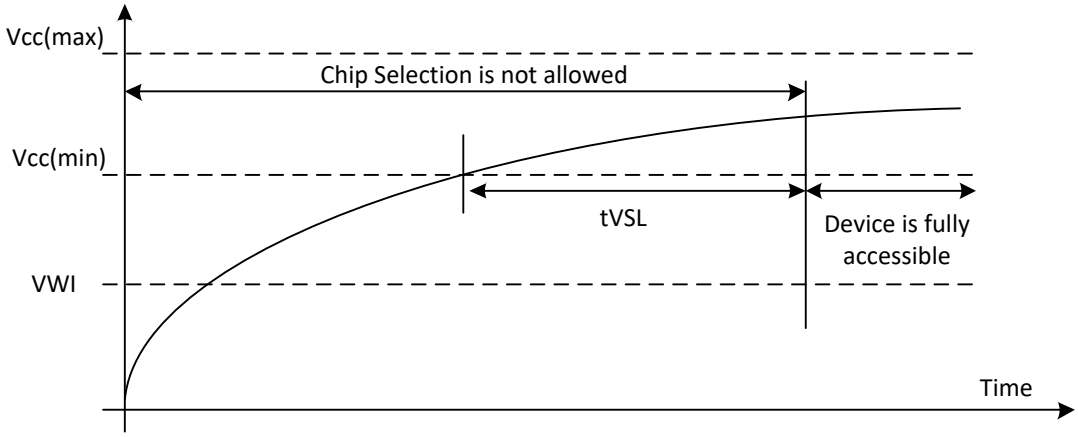
The Enable Reset (66H) command must be issued prior to a Reset (99H) command and any other commands can't be inserted between them. Otherwise, Enable Reset (66H) command will be cleared.

**Figure 29. Enable Reset and Reset command Sequence Diagram**



# 7. ELECTRICAL CHARACTERISTICS

## 7.1. Power-on Timing




**Power-Up Timing and Write Inhibit Threshold**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VSL}$ | VCC(min) To CS# Low | 100 | | us |
| $V_{WI}$ | Write Inhibit Voltage | 1.5 | 2.5 | V |

## 7.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). All Status Register bits except S22 bits are 0, S22 bit is 1.

## 7.3. Latch up Characteristics

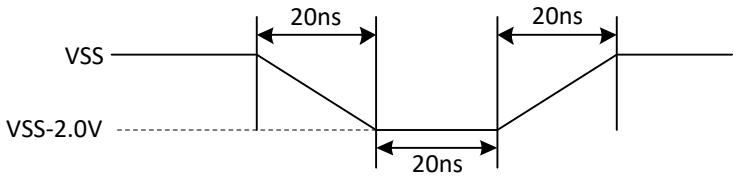
| Parameter | Min | Max |
|---|---|---|
| Input Voltage Respect To VSS On I/O Pins | -1.0V | VCC+1.0V |
| VCC Current | -100mA | 100mA |

## 7.4. Absolute Maximum Ratings

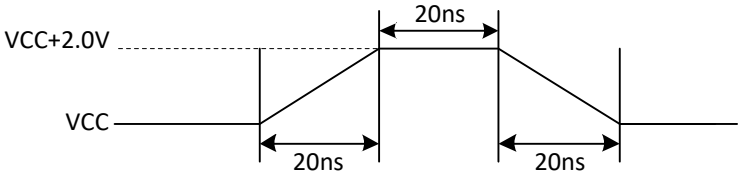
| Parameter | Value | Unit |
|---|---|---|
| Ambient Operating Temperature | -40 to 85 | °C |
| Storage Temperature | -65 to 150 | °C |
| Output Short Circuit Current | 200 | mA |
| Applied Input/Output Voltage | -0.5 to 4.0 | V |
| VCC | -0.5 to 4.0 | V |

**Input Test Waveform and Measurement Level**

**Maximum Negative Overshoot Waveform**



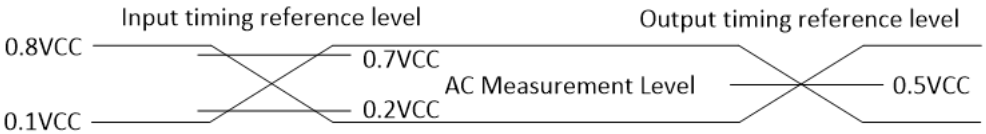

**Maximum Positive Overshoot Waveform**




## 7.5. Capacitance Measurement Condition

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 6 | pF | VIN=0V |
| COUT | Output Capacitance | | | 8 | pF | VOUT=0V |
| CL | Load Capacitance | 30 | | | pF | |
| | Input Rise And Fall time | | | 5 | ns | |
| | Input Pulse Voltage | 0.1VCC to 0.8VCC | | | V | |
| | Input Timing Reference Voltage | 0.2VCC to 0.7VCC | | | V | |
| | Output Timing Reference Voltage | | 0.5VCC | | V | |

**Absolute Maximum Ratings Diagram**




Note: Input pulse rise and fall time are <5ns

## 7.6. DC Characteristics

(TA=-40°C ~85°C,VCC=2.7~3.6V)

| Symbol | Parameter | Test Condition | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| ILI | Input Leakage Current | | | | ±2 | µA |
| ILO | Output Leakage Current | | | | ±2 | µA |
| ICC1 | Standby Current | CS#=VCC<br>VIN=VCC or VSS | | 15 | 55 | µA |
| ICC2 | Deep Power-Down Current | CS#=VCC<br>VIN=VCC or VSS | | 0.3 | 8 | µA |
| ICC3 | Operating Current(Read) | CLK=0.1VCC/0.9VCC at 133MHz,Q=Open(*1,*2,*4 I/O) | | 12 | 20 | mA |
| | | CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O) | | 9 | 13 | mA |
| ICC4 | Operating Current(PP) | CS#=VCC | | | 40 | mA |
| ICC5 | Operating Current(WRSR) | CS#=VCC | | | 25 | mA |
| ICC6 | Operating Current(SE) | CS#=VCC | | | 25 | mA |
| ICC7 | Operating Current(BE) | CS#=VCC | | | 25 | mA |
| ICC8 | Operating Current(CE) | CS#=VCC | | | 25 | mA |
| VIL | Input Low Voltage | | -0.5 | | 0.2VCC | V |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.4 | V |
| VOL | Output Low Voltage | IOL=100uA | | | 0.2 | V |
| VOH | Output High Voltage | IOH=-100uA | VCC-0.2 | | | V |

**Note:**

1. Typical values given for TA=25°C, VCC=3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

## 7.7. AC Characteristics

(TA=-40°C ~85°C,VCC=2.7~3.6V， $C_L$=30pF)

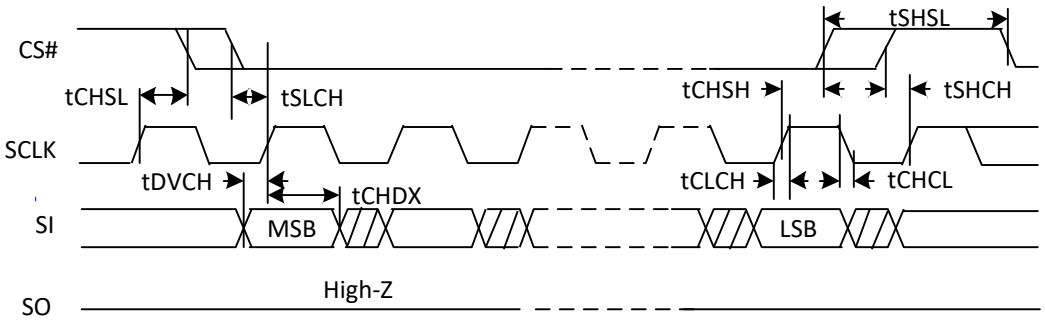
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| fC | Serial Clock Frequency For: all commands except Read (03H), on 3.0-3.6V power supply, DC=1. | | | 133 | MHz |
| fC1 | Serial Clock Frequency For: all commands except Read (03H), on 2.7-3.0V power supply, DC=1. | | | 104 | MHz |
| fC2 | Serial Clock Frequency For: all commands except Read (03H), DC=0 | | | 104 | MHz |
| fR | Serial Clock Frequency For: Read (03H) | | | 80 | MHz |
| tCLH | Serial Clock High Time | 45% PC | | | ns |
| tCLL | Serial Clock Low Time | 45% PC | | | ns |
| tCLCH | Serial Clock Rise Time(Slew Rate) | 0.2 | | | V/ns |
| tCHCL | Serial Clock Fall Time(Slew Rate) | 0.2 | | | V/ns |
| tSLCH | CS# Active Setup Time | 5 | | | ns |
| tCHSH | CS# Active Hold Time | 5 | | | ns |
| tSHCH | CS# Not Active Setup Time | 5 | | | ns |
| tCHSL | CS# Not Active Hold Time | 5 | | | ns |
| tSHSL | CS# High Time (read/write) | 20 | | | ns |
| tSHQZ | Output Disable Time | | | 6 | ns |
| tCLQX | Output Hold Time | 1 | | | ns |
| tCLQV | Clock Low To Output Valid | | | 5.5 | ns |
| tDVCH | Data In Setup Time | 2 | | | ns |
| tCHDX | Data In Hold Time | 2 | | | ns |
| tHLCH | Hold# Low Setup Time(relative to Clock) | 5 | | | ns |
| tHHCH | Hold# High Setup Time(relative to Clock) | 5 | | | ns |
| tCHHL | Hold# High Hold Time(relative to Clock) | 5 | | | ns |
| tCHHH | Hold# Low Hold Time(relative to Clock) | 5 | | | ns |
| tHLQZ | Hold# Low To High-Z Output | | | 6 | ns |
| tHHQX | Hold# High To Low-Z Output | | | 6 | ns |
| tWHSL | Write Protect Setup Time Before CS# Low | 20 | | | ns |
| tSHWL | Write Protect Hold Time After CS# High | 100 | | | ns |
| tDP | CS# High To Deep Power-Down Mode | | | 3 | µs |
| tRES1 | CS# High To Standby Mode Without Electronic Signa-ture Read | | | 20 | µs |
| tRES2 | CS# High To Standby Mode With Electronic Signature Read | | | 20 | µs |
| tRST_R | CS# High To Next Command After Reset (from read) | | | 30 | µs |

| | | | | | |
|---|---|---|---|---|---|
| tRST_P | CS# High To Next Command After Reset (from program) | | | 30 | µs |
| tRST_E | CS# High To Next Command After Reset (from erase) | | | 12 | ms |
| tW | Write Status Register Cycle Time | | 3 | 20 | ms |
| tPP | Page Programming Time | | 0.4 | 2 | ms |
| tSE | Sector Erase Time | | 50 | 2000 | ms |
| tBE1 | Block Erase Time(32K Bytes) | | 0.15 | 2.2 | s |
| tBE2 | Block Erase Time(64K Bytes) | | 0.25 | 2.5 | s |
| tCE | Chip Erase Time | | 12 | 30 | s |

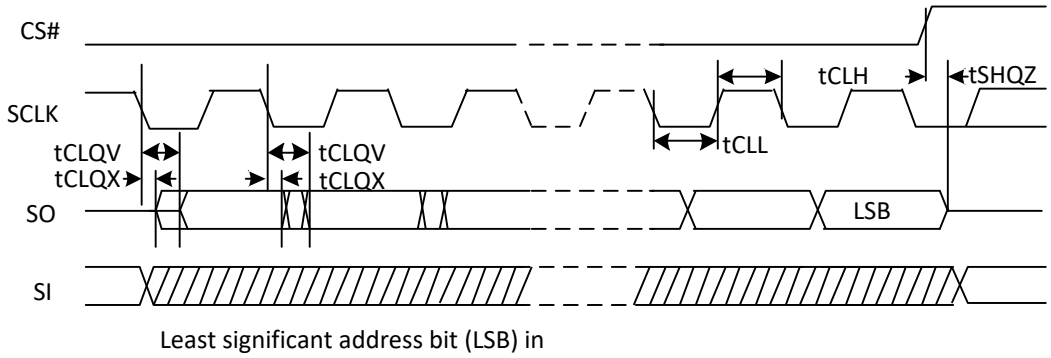
**Note:**

1. Clock high or Clock low must be more than or equal to 45%PC. PC=1/fC(MAX).
2. Typical values given for TA=25°C, VCC=3.3V. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Maximum Sector Erase Time at 40K P/E cycle is 1200ms.

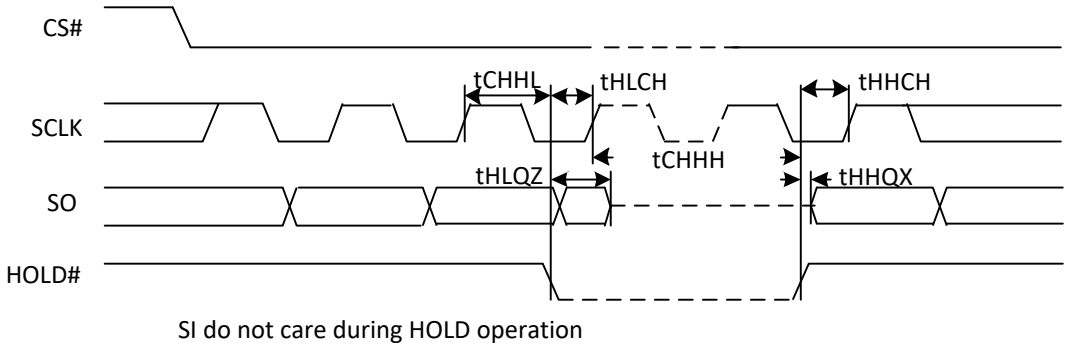
**Serial Input Timing**




**Output Timing**




**Hold Timing**



# 8. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following

**XT 25F 32F SO I G U**

## Company Prefix

**XT = XTX**

## Product Family

**25F** = 2.7~3.6V Serial Flash Memory
with 4KB Uniform-Sector

## Product Density

**32F** = 32M bit

## Product Package

**SO** = SOP8 150mil
**SS** = SOP8 208mil
**DT** = DFN8 (2x3x0.4mm)

## Temperature & Moisture Sensitivity Level

**I** = Industrial Level Temperature. (-40℃ to +85℃), MSL3

## Green Code

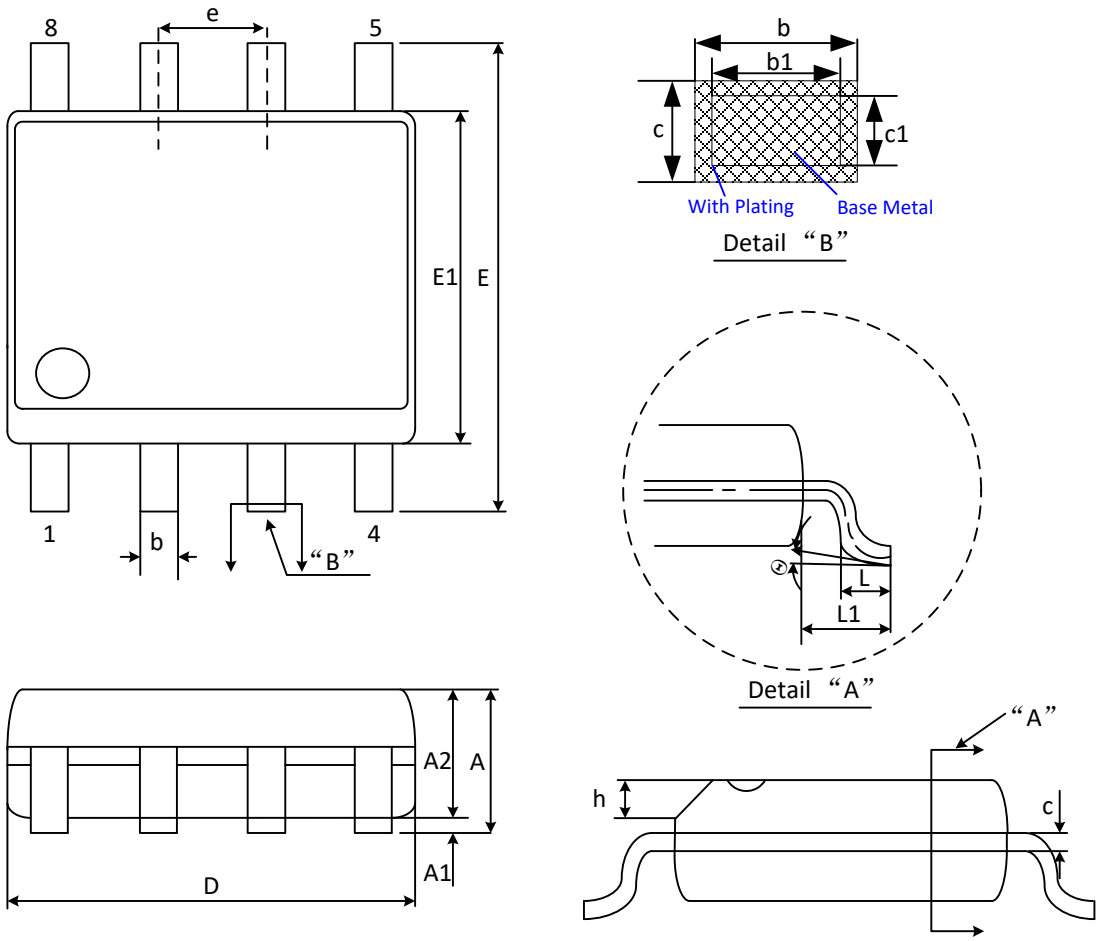
**G** = Green/Reach Package

## Product Carrier

**U** = Tube; **T** = Tape & Reel; **A** = Tray

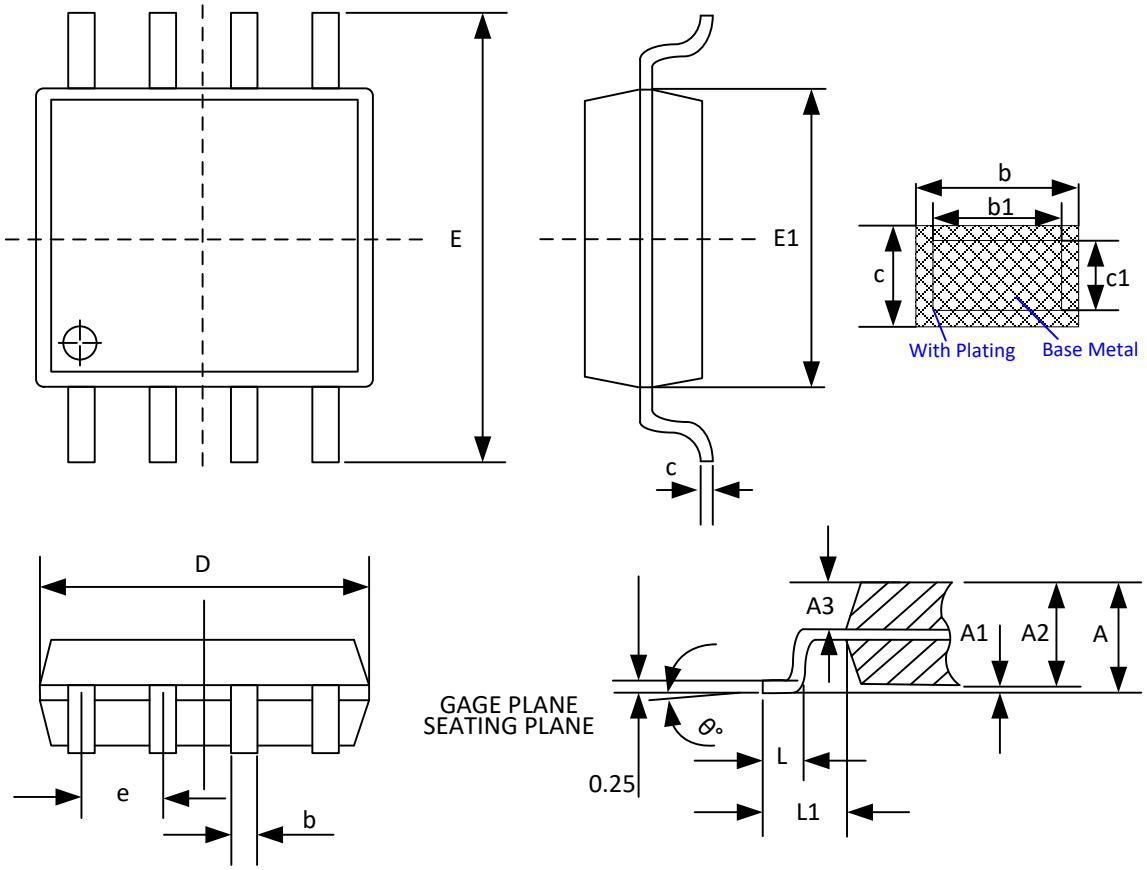
# 9. PACKAGE INFORMATION

## 9.1. Package SOP8 150mil



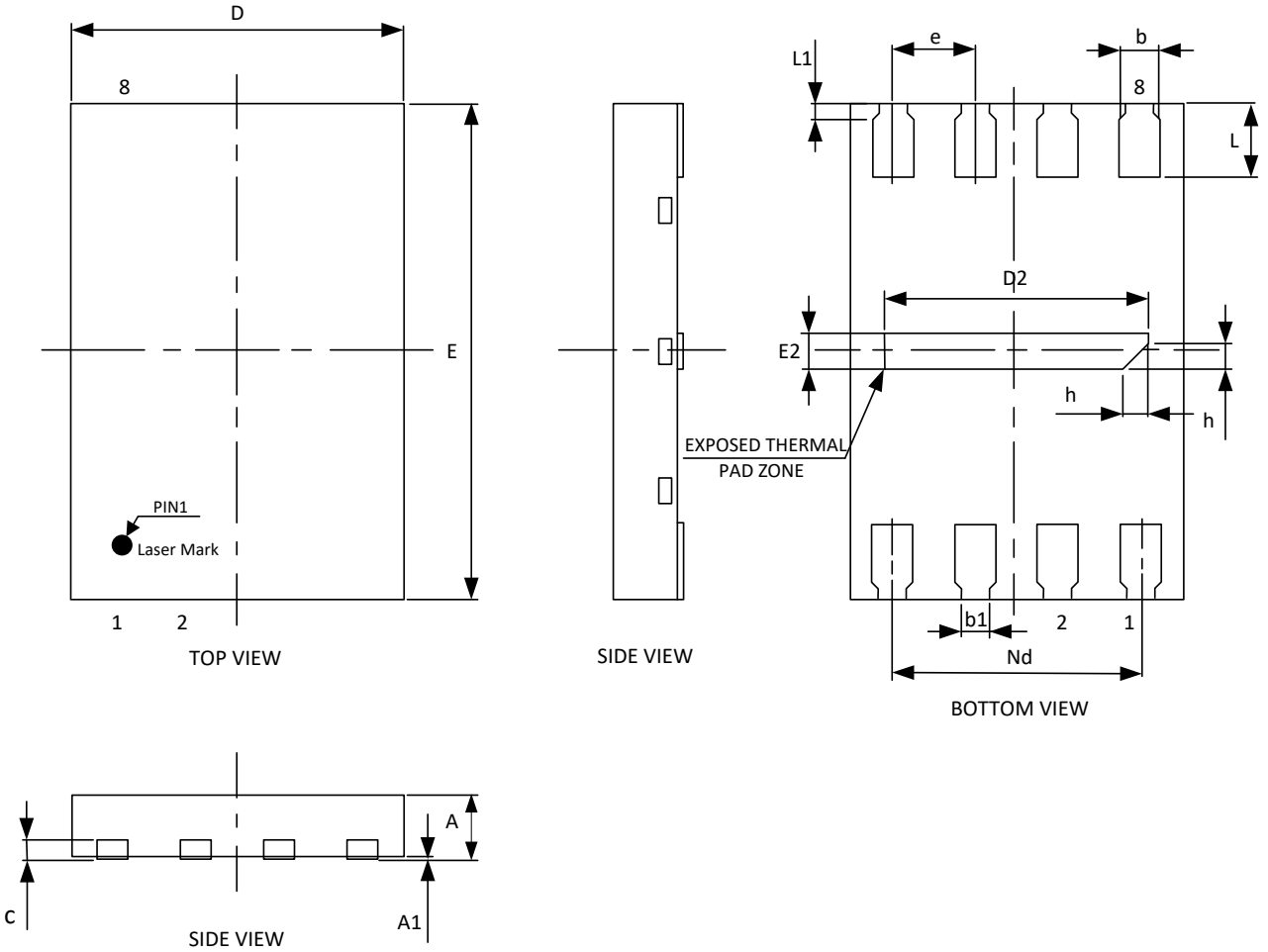

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.75 |
| A1 | 0.10 | — | 0.25 |
| A2 | 1.30 | 1.40 | 1.50 |
| b | 0.39 | — | 0.47 |
| b1 | 0.38 | 0.41 | 0.44 |
| c | 0.20 | — | 0.24 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 4.80 | 4.90 | 5.00 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27BSC | | |
| E | 5.80 | 6.00 | 6.20 |
| h | 0.25 | — | 0.50 |
| L | 0.50 | — | 0.80 |
| L1 | 1.05REF | | |
| θ | 0° | — | 8° |

## 9.2. Package SOP8 208mil




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| **A** | 1.75 | 1.95 | 2.15 |
| **A1** | 0.05 | 0.15 | 0.25 |
| **A2** | 1.70 | 1.80 | 1.90 |
| **A3** | 0.75 | 0.80 | 0.85 |
| **b** | 0.33 | — | 0.51 |
| **b1** | 0.30 | — | 0.48 |
| **c** | 0.17 | — | 0.25 |
| **c1** | 0.15 | 0.20 | 0.23 |
| **D** | 5.13 | 5.23 | 5.33 |
| **E** | 7.70 | 7.90 | 8.10 |
| **E1** | 5.18 | 5.28 | 5.38 |
| **e** | 1.27 BSC | | |
| **L** | 0.50 | 0.65 | 0.80 |
| **L1** | 1.31 REF | | |
| **θ** | 0° | — | 8° |

## 9.3. Package DFN8 (2x3x0.4) mm




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.35 | — | 0.40 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| b1 | 0.18REF | | |
| c | 0.127REF | | |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.50 | 1.60 | 1.70 |
| e | 0.50BSC | | |
| Nd | 1.50BSC | | |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 0.10 | 0.20 | 0.30 |
| L | 0.40 | 0.45 | 0.50 |
| L1 | 0.05 | 0.10 | 0.15 |
| h | 0.10 | 0.15 | 0.20 |

# 10. REVISION HISTORY

| Revision | Description | Date |
|---|---|---|
| 1.0 | Initial Version | Dec 8, 2021 |