XT25F04B

Single IO Serial NOR Flash Datasheet

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Serial NOR Flash Memory

4M bits 3V Single I/O Serial Flash Memory with 4KB Uniform Sector

- **4M -bit Serial Flash**
  - 512 K-byte
  - 256 bytes per programmable page
- **Standard, Dual SPI**
  - Standard SPI: SCLK, CS#, SI, SO
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 64k-byte
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40℃ to +85℃), MSL3
- **Software Write Protection**
  - Write protect all/portion of memory via software
- **Low Power Consumption**
  - 10mA maximum active current
  - 5uA maximum Standby current
- **Single Power Supply Voltage: Full voltage range:**
  - 2.7~3.6V
- **Minimum 100,000 Program/Erase Cycle**
- **Support 128 bits Unique ID**
- **High Speed Clock Frequency**
  - 120MHz for fast read with 30PF load
- **Program/Erase Speed**
  - Page Program time: 1.5ms typical
  - Sector Erase time: 150ms typical
  - Block Erase time: 0.8s typical
  - Chip Erase time: 6s typical

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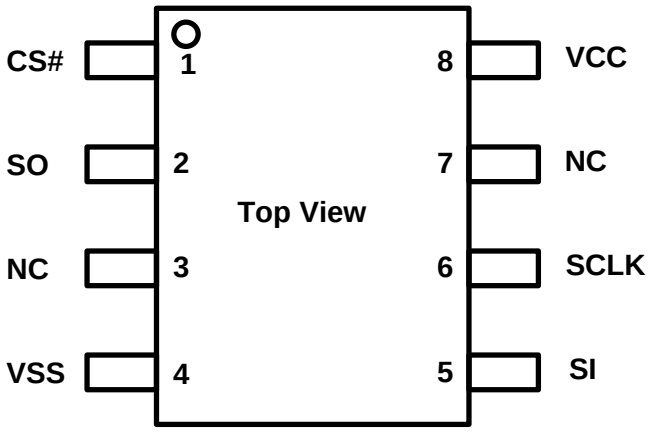
1. GENERAL DESCRIPTION

The XT25F04B (4M) bits Serial flash supports the standard Serial Peripheral Interface (SPI). SPI clock frequency of up to 120MHz is supported for fast read command.

1.1. Available Ordering OPN

OPN	Package Type	Package Carrier
XT25F04BSOIGU	SO8 150mil	Tube
XT25F04BSOIGT	SO8 150mil	Tape & Reel
XT25F04BSOIGA	SO8 150mil	Tray
XT25F04BSSIGU	SO8 208mil	Tube
XT25F04BSSIGT	SO8 208mil	Tape & Reel
XT25F04BTSIGU	TSSOP8	Tube
XT25F04BTSIGT	TSSOP8	Tape & Reel
XT25F04BDFIGT	DFN8 2x3x0.55mm	Tape & Reel

1.2. Connection Diagram

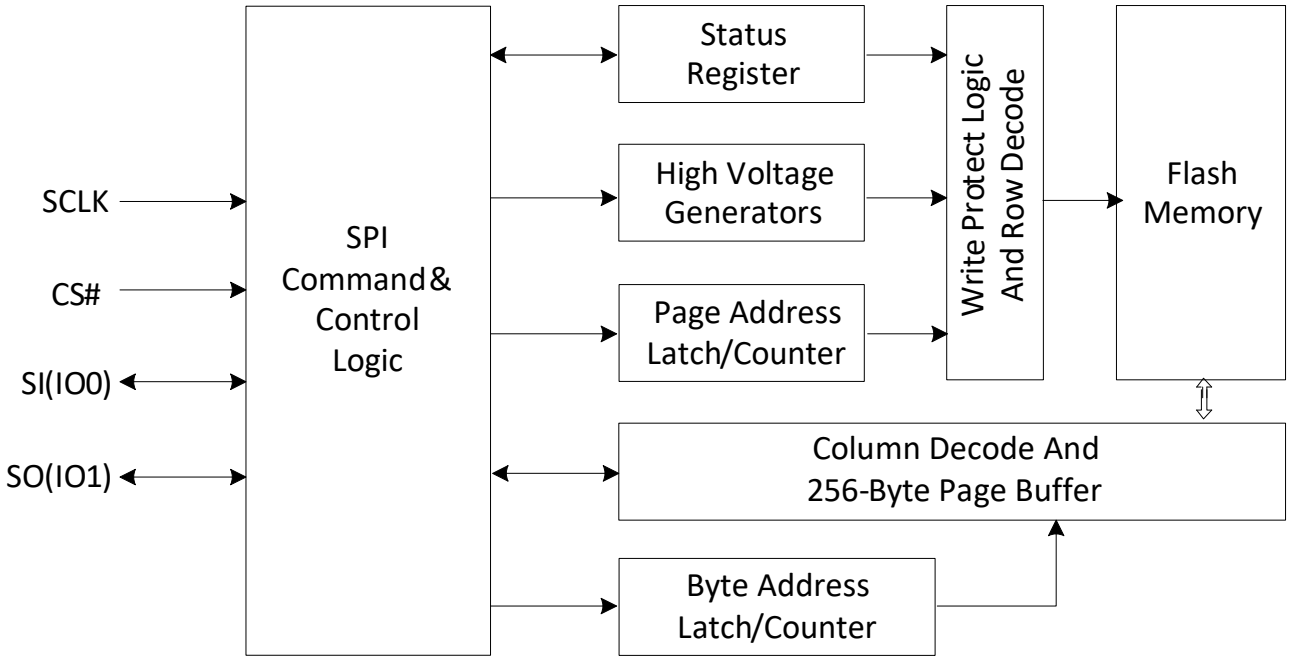


8 – LEAD SOP / DFN8

1.3. Pin Description

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	O	Data Output
VSS		Ground
SI (IO0)	I	Data Input
SCLK	I	Serial Clock Input
VCC		Power Supply

1.4. Block Diagram



2. MEMORY ORGANIZATION

XT25F04B Memory Description

Each Device has	Each block has	Each sector has	Each page has	
512K	64K	4K	256	bytes
2K	256	16	-	pages
128	16	-	-	sectors
8	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

XT25F04B 64K Bytes Block Sector Architecture

Block	Sector	Address range	
7	127	07F000H	07FFFFH
	……	……	……
	112	070000H	070FFFH
6	111	06F000H	06FFFFH
	……	……	……
	96	060000H	060FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

3. DEVICE OPERATION

The XT25F04B features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

4. DATA PROTECTION

The XT25F04B provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode:
  - SRWD=0, the Block Protect (BP2, BP1, BP0) bits define the section of the memory array that can be read but not change
  - SRWD=1, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP2, BP1, BP0) are read only.

Table1.0 XT25F04B Protected Area Sizes

Status bit			Protect level	Protect Block
BP2	BP1	BP0		
0	0	0	0(none)	None
0	0	1	1 (1 block)	Block 7
0	1	0	2 (2 blocks)	Block 6-7
0	1	1	3 (4 blocks)	Block 4-7
1	0	0	4 (8 blocks)	All
1	0	1	5 (All)	All
1	1	0	6 (All)	All
1	1	1	7 (All)	All

5. STATUS REGISTER

S7	S6	S5	S4	S3	S2	S1	S0
SRWD	Reserved	Reserved	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP2, BP1, BP0 bits.

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1.0) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. Chip Erase command will be ignored if one or more of the Block Protect (BP2, BP1, BP0) bits are 1.

SRWD bit.

The Status Register Write Disable (SRWD) bit is a non-volatile One Time Program(OTP) bit in the status register that provide another software protection. Once it is set to 1, the Write Status Register (WRSR) instruction is no longer accepted and the SRWD bit and Block Protect bits (BP2, BP1, BP0) are read only.

SRWD	Status register	Memory
0	Status register can be written in (WEL bit is set to "1") and the SRWD, BP2-BP0 bits can be changed	The protected area cannot be program or erase
1	The SRWD, BP2-BP0 of status register bits cannot be changed	The protected area cannot be program or erase

6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable or Write Disable command, CS# must be driven high exactly at the byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Write Enable for Volatile Status Register	50H						
Read Status Register	05H	(S7-S0)					(continuous)
Write Status Register	01H	(S7-S0)					(continuous)
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Read Unique ID	90H	00H	00H	00H	Dummy (1)	Dummy (2)	Dummy..(16) D0..D7
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)

Table of ID Definitions:

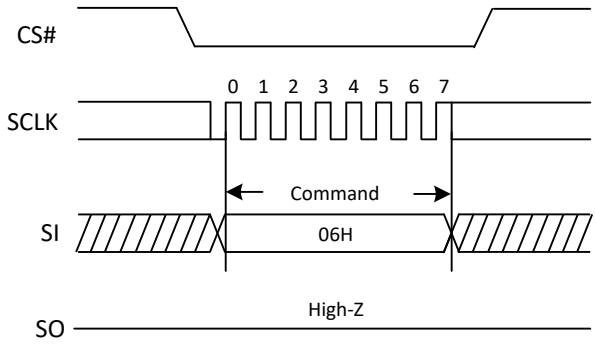
XT25F04B

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0B	40	13
90H	0B		12

6.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low→sending the Write Enable command→CS# goes high.

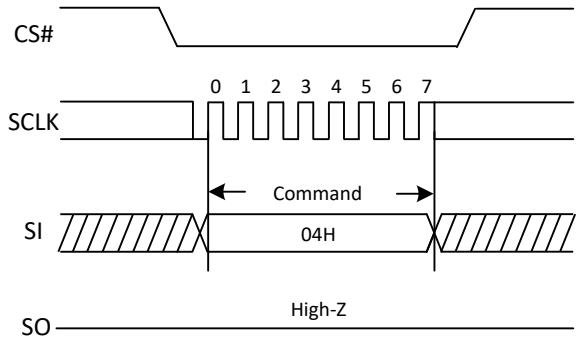
Figure1. Write Enable Sequence Diagram



6.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→sending the Write Disable command→CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

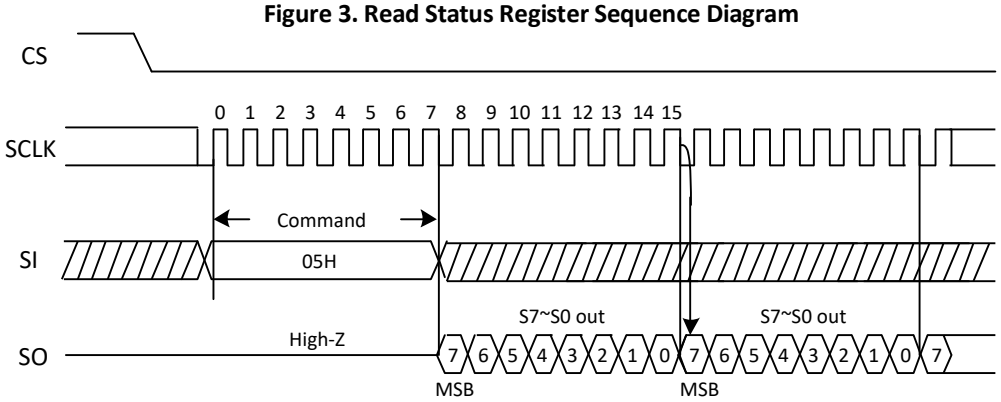
Figure 2. Write Disable Sequence Diagram



6.3. Read Status Register (RDSR) (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously.

Figure 3. Read Status Register Sequence Diagram



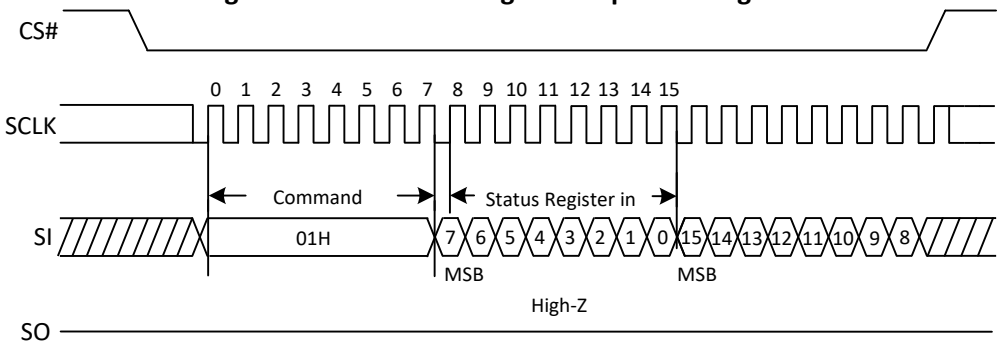
6.4. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1.0. The Status Register Write Disable (SRWD) bit is a non-volatile One Time Program(OTP) bit, the Write Status Register (WRSR) command allows the user to set the Status Register Write Disable (SRWD) bit to 1. The Status Register Write Disable (SRWD) bit allow the device to be put in another Software Protected Mode. Once the SRWD bit is set to 1, the Write Status Register (WRSR) command is not executed, and the SRWD bit and Block Protect bits (BP2, BP1, BP0) are read only.

The Write Status Register (WRSR) command has no effect on S6, S5, S1 and S0 of the Status Register. CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

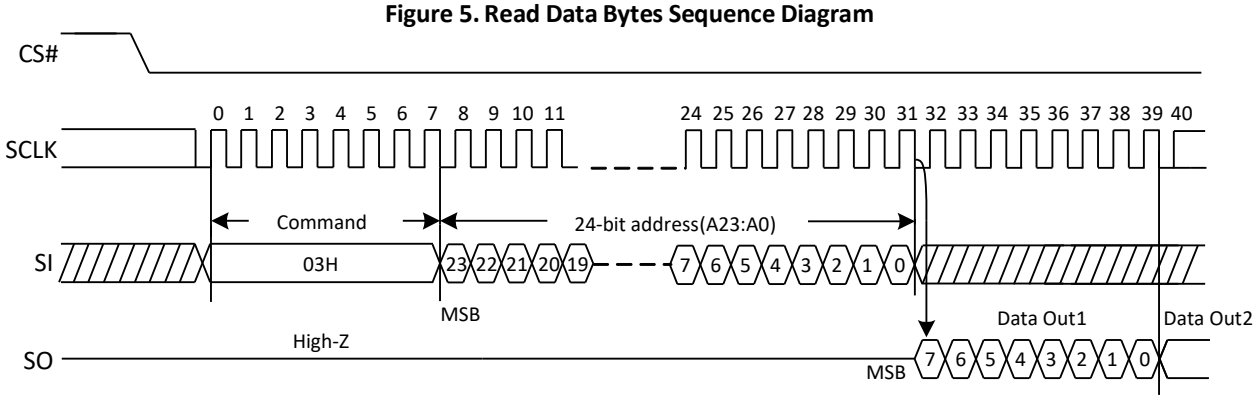
Figure 4. Write Status Register Sequence Diagram



6.5. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

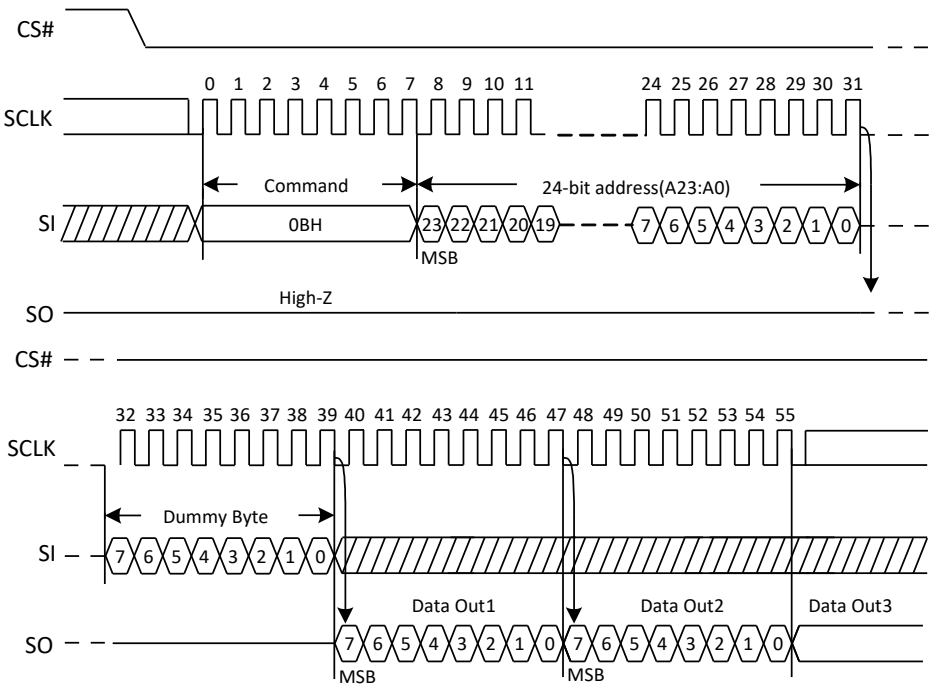
Figure 5. Read Data Bytes Sequence Diagram



6.6. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for fast reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 6. Read Data Bytes at Higher Speed Sequence Diagram



6.7. Page Program (PP) (02H)

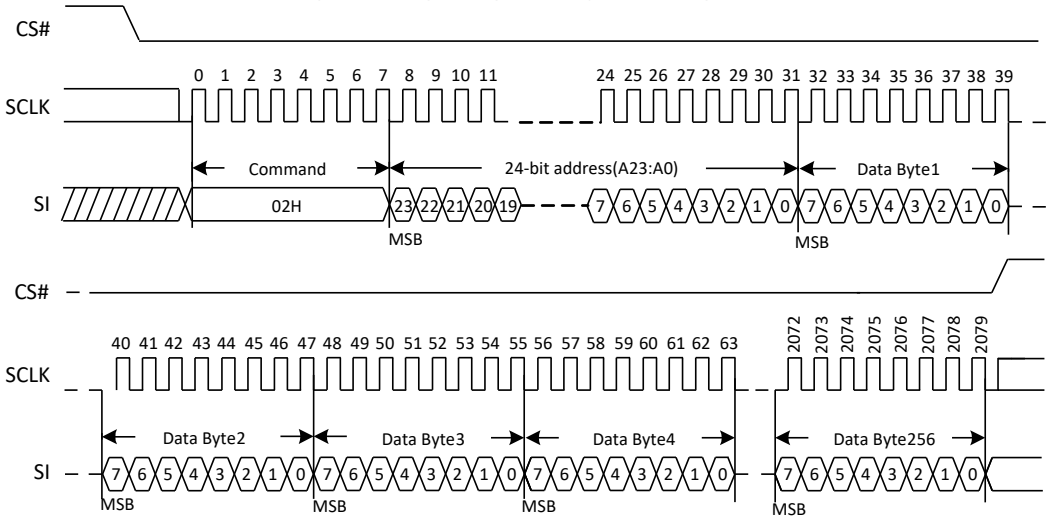
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure 7. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP1, BP0) is not executed.

Figure 7. Page Program Sequence Diagram



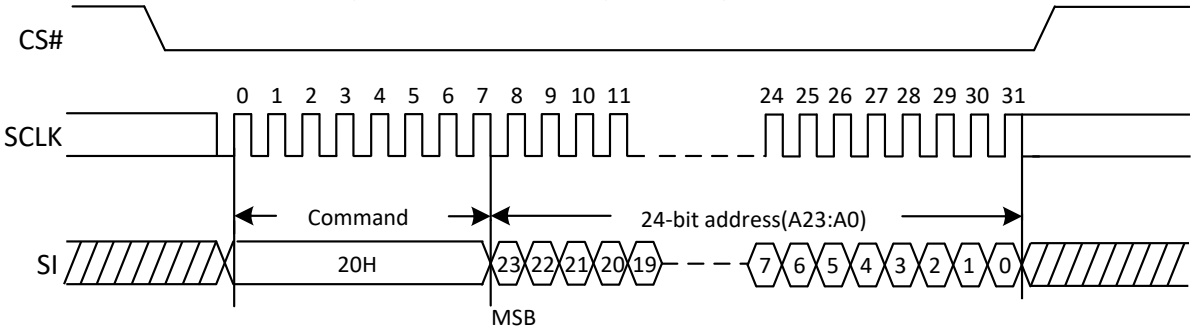
6.8. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low →sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 8. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated.

While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bit (see Table1.0) is not executed.

Figure 8. Sector Erase Sequence Diagram

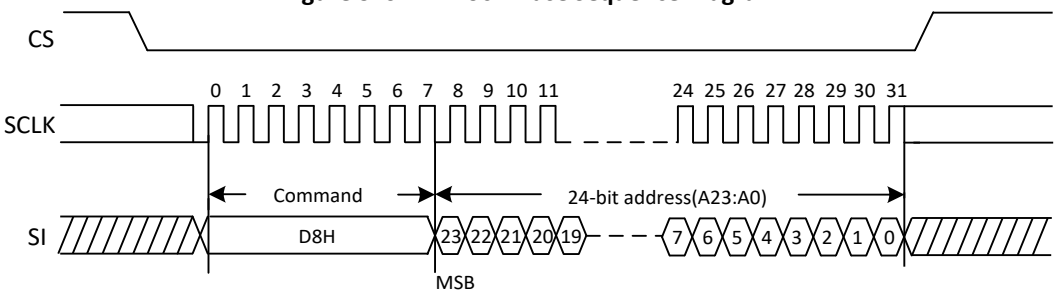


6.9. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command →3byte address on SI → CS# goes high. The command sequence is shown in Figure 9. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. Write Enable Latch (WEL) bit is reset to 0 at the end of the Block Erase cycle. Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table1.0) is not executed.

Figure 9. 64KB Block Erase Sequence Diagram

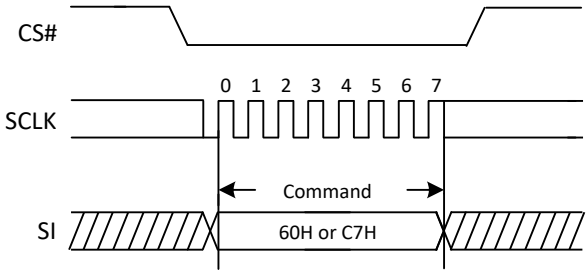


6.10. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure 10. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. Write Enable Latch (WEL) bit is reset to 0 at the end of the Chip Erase cycle. The Chip Erase (CE) command is ignored if one or more sectors are protected by (BP2, BP1, BP0) bits.

Figure 10. Chip Erase Sequence Diagram

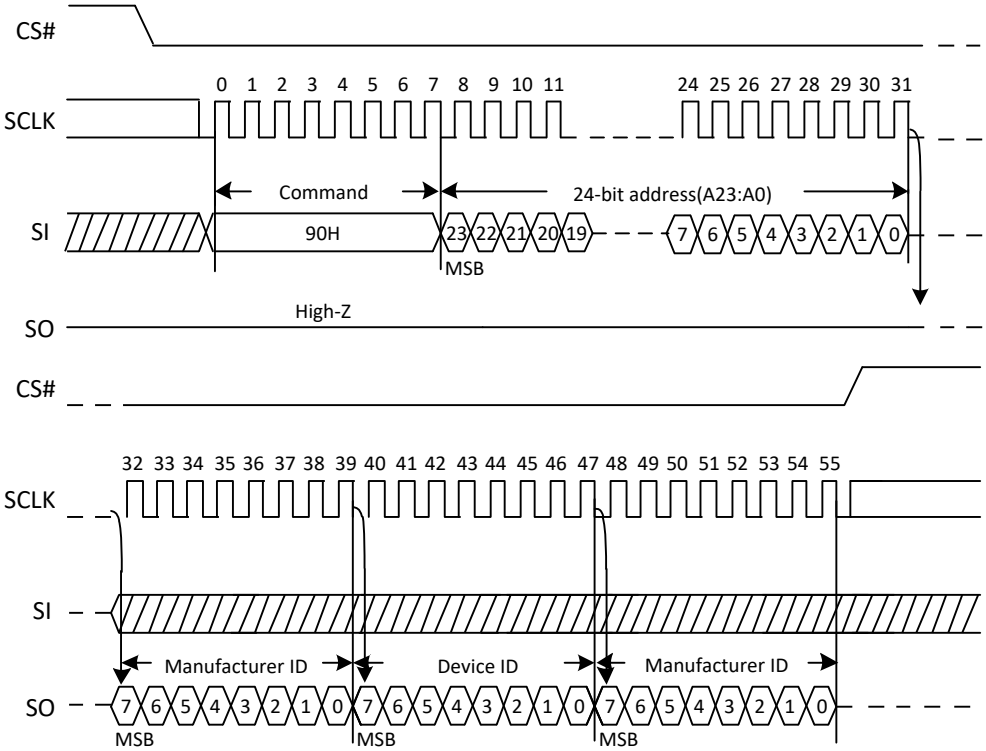


6.11. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 11. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 11. Read ID Sequence Diagram



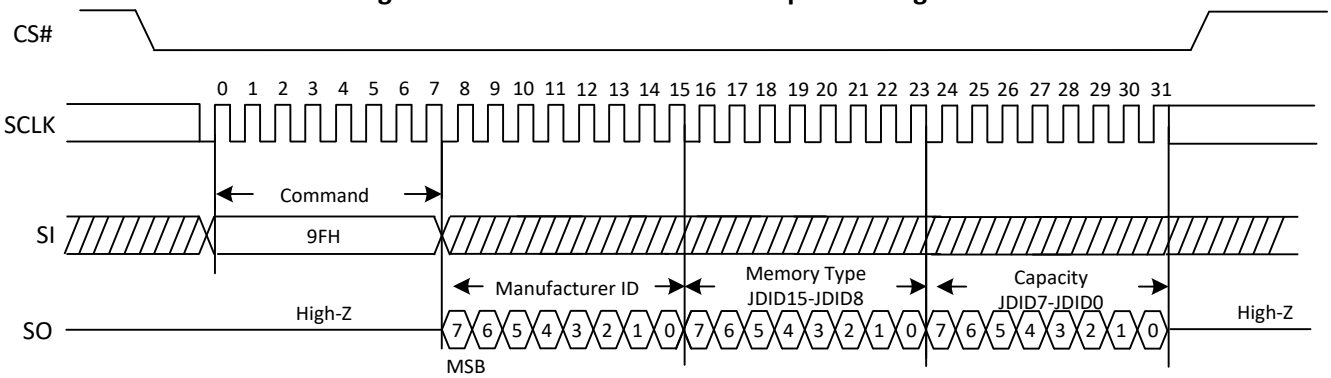
6.12. Read Unique ID (RUID) (90H)

Please contact XTX FAE for detail

6.13. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure 12. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. After CS# is driven high, the device returns to Standby Mode and awaits for new command.

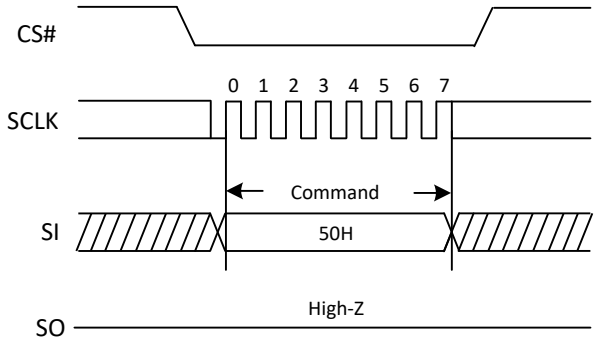
Figure 12. Read Identification ID Sequence Diagram



6.14. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 13. Write Enable for Volatile Status Register Sequence Diagram



7. ELECTRICAL CHARACTERISTICS

7.1. Power-on Timing

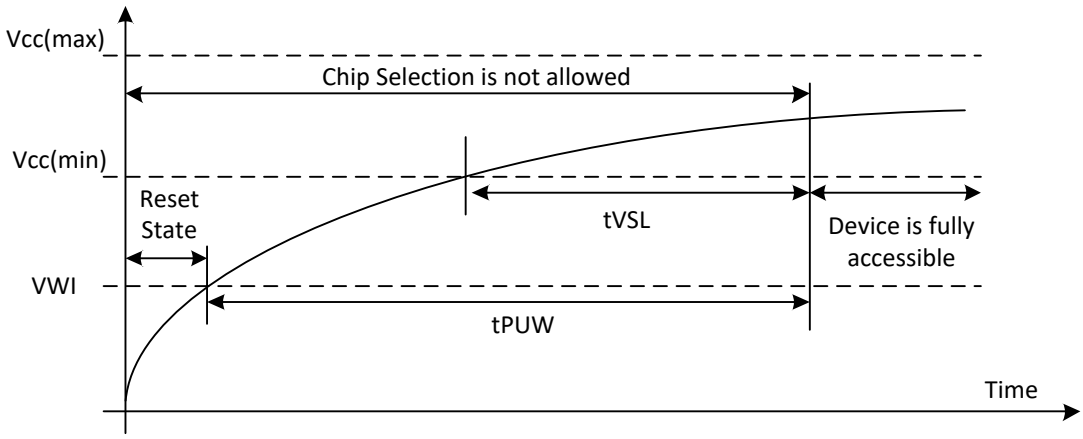


Table3. Power-Up Timing and Write Inhibit Threshold

Note: At power-down, need to ensure VCC drop to 0.5V before the next power-on in order for the device to have a proper power-on reset.

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC(min) To CS# Low	10		us
t_{PUW}	Time Delay Before Write Instruction	1	-	ms
V_{WI}	Write Inhibit Voltage	1.5	2.5	V

7.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

7.3. Data Retention and Endurance

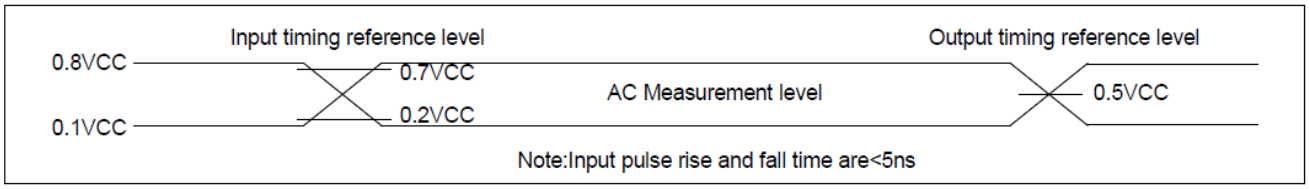
Parameter	Typical	Unit
Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

7.4. Latch up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

7.5. Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

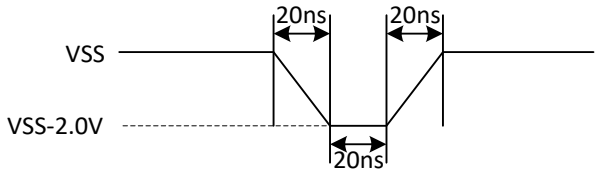


7.6. Capacitance Measurement Condition

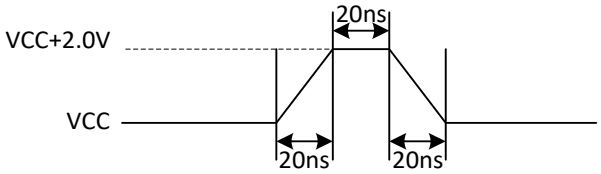
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 14. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



7.7. DC Characteristics

(T=-40℃~85℃,VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
ILI	Input Leakage Current				±2	µA
ILO	Output Leakage Current				±2	µA
ICC1	Standby Current	CS#=VCC VIN=VCC or VSS		1	5	µA
ICC3	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 120MHz for Fast Read		15	20	mA
		CLK=0.1VCC/0.9VCC at 40MHz for Read		13	18	mA
ICC4	Operating Current(PP)	CS#=VCC			20	mA
ICC5	Operating Current(WRSR)	CS#=VCC			20	mA
ICC6	Operating Current(SE)	CS#=VCC			20	mA
ICC7	Operating Current(BE)	CS#=VCC			20	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.7VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL=1.6mA			0.4	V
VOH	Output High Voltage	IOH=-100uA	VCC-0.2			V

7.8. AC Characteristics

(T=-40℃~85℃,VCC=2.7~3.6V， C_L=30pF)

Symbol	Parameter	Min.	Typ	Max.	Unit
f_C	Serial Clock Frequency For:Fast Read(0BH),			120	MHz
f_R	Serial Clock Frequency For:Read(03H)			40	MHz
t_{CLH}	Serial Clock High Time	4			ns
t_{CLL}	Serial Clock Low Time	4			ns
t_{CLCH}	Serial Clock Rise Time(Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time(Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (read/write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	Hold# Low Setup Time(relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time(relative to Clock)	5			ns
t_{CHHL}	Hold# High Hold Time(relative to Clock)	5			ns
t_{CHHH}	Hold# Low Hold Time(relative to Clock)	5			ns
t_{HLQZ}	Hold# Low To High-Z Output			6	ns
t_{HHQX}	Hold# Low To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid			6.5	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			0.1	us
t_W	Write Status Register Cycle Time		100	200	ms
t_{PP}	Page Programming Time		1.5	5	ms
t_{SE}	Sector Erase Time		120	300	ms
t_{BE}	Block Erase Time		0.8	1.5	s
t_{CE}	Chip Erase Time		6	10	s

Max Value 4KB t_{SE} with<50K cycles is 180ms and >50K & <100k cycles is 300ms.
Max Value 64KB t_{BE} with<50K cycles is 1.1s and >50K & <100k cycles is 1.5s.
The value guaranteed by characterization, not 100% tested in production.

Figure 15. Serial Input Timing

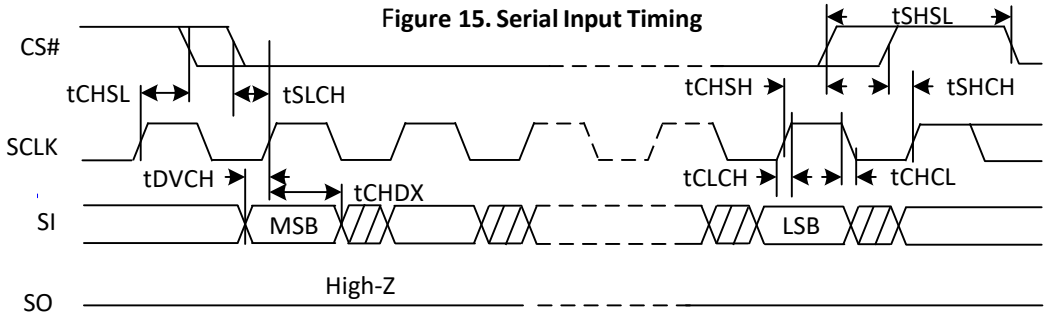
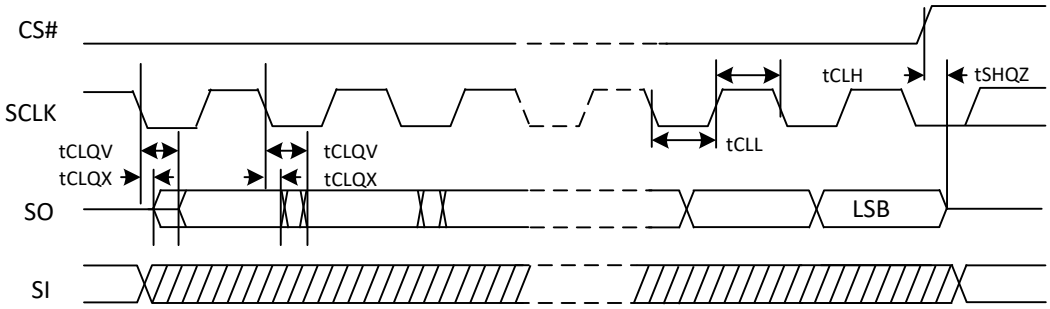


Figure 16. Output Timing



Least significant address bit (LSB) in

8. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following

XT 25F 04B SO I G U

Company Prefix

XT = XTX

Product Family

25F = 2.7~3.6V Serial Flash Memory with
4KB Uniform-Sector

Product Density

04B = 4M bit

Product Package

SO = 8-pin SOP8(150mil)
SS = 8-pin SOP8(208mil)
TS = 8-pin TSSOP8
DF = 8-pad DFN8(2x3x0.55mm)
VS = 8-pin VSOP8 (208mil)

Temperature & Moisture Sensitivity Level

I = Industrial Level Temp. (-40℃ to +85℃), MSL3
H = Industrial Plus Level Temp. (-40℃ to +105℃), MSL1

Green Code

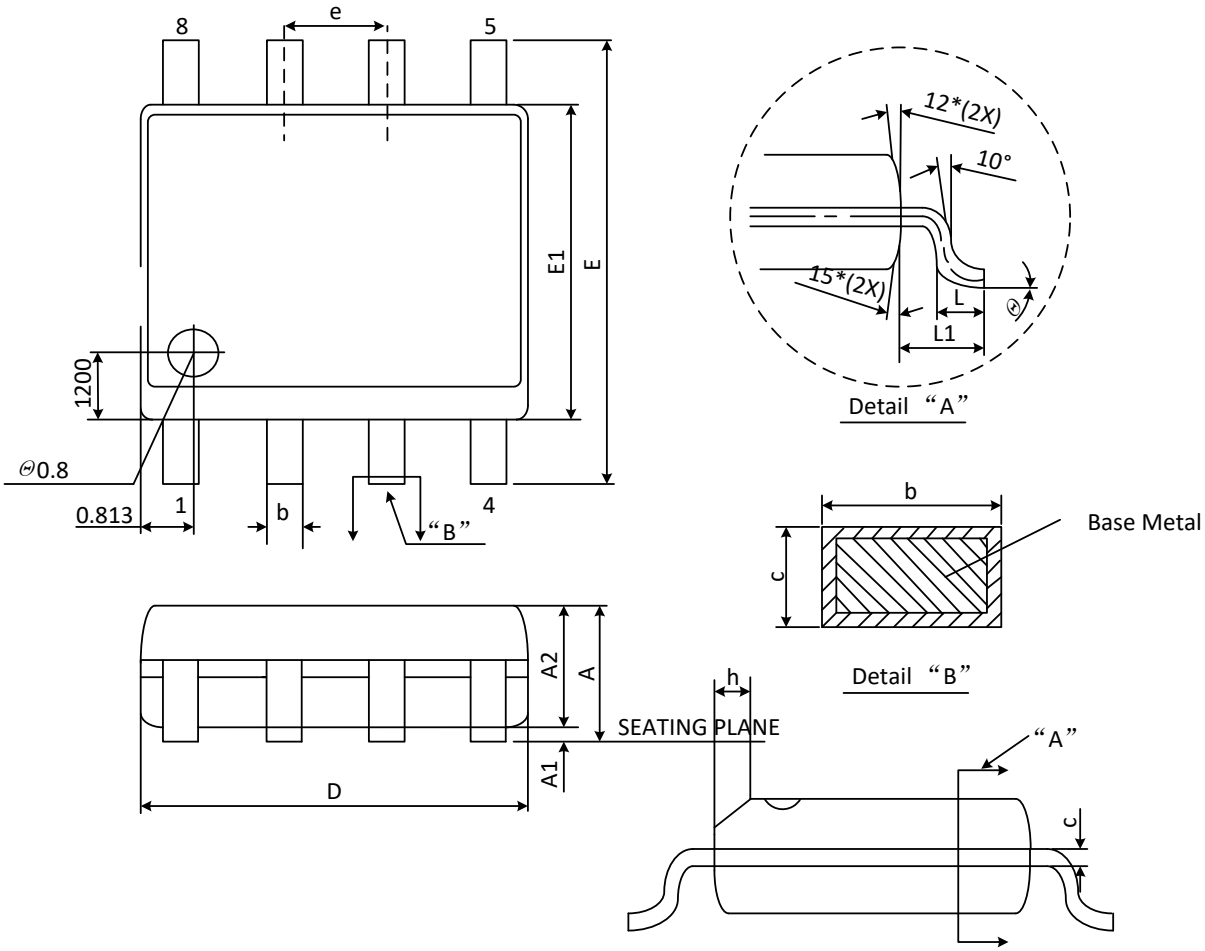
G = Green/Reach Package

Product Carrier

U = Tube; **T** = Tape & Reel; **A** = Tray

9. PACKAGE INFORMATION

9.1. Package SOP8 150MIL

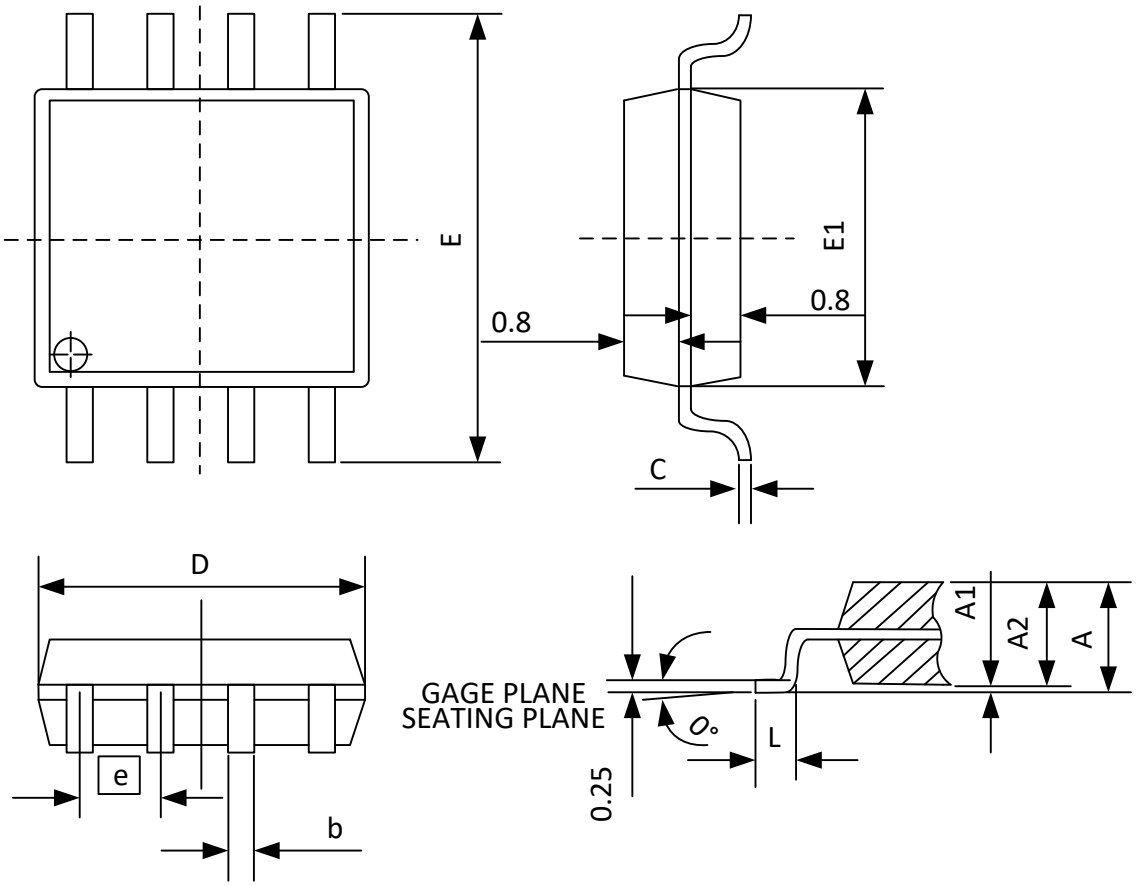


Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	1.350	----	1.750
A1	0.100	----	0.250
A2	1.300	----	1.500
b	0.330	----	0.510
c	0.190	----	0.250
D	4.700	4.900	5.000
E1	3.800	3.900	4.000
e	----	1.270	----
E	5.800	6.000	6.200
h	0.2500	0.350	0.500
L	0.508	0.635	0.762
L1	0.837	1.040	1.243
θ	0°	----	8°

Note:

1. Coplanarity: 0.1mm
2. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.
3. All dimensions follow JEDEC MS-012 standard.

9.2. Package SOP8 208MIL

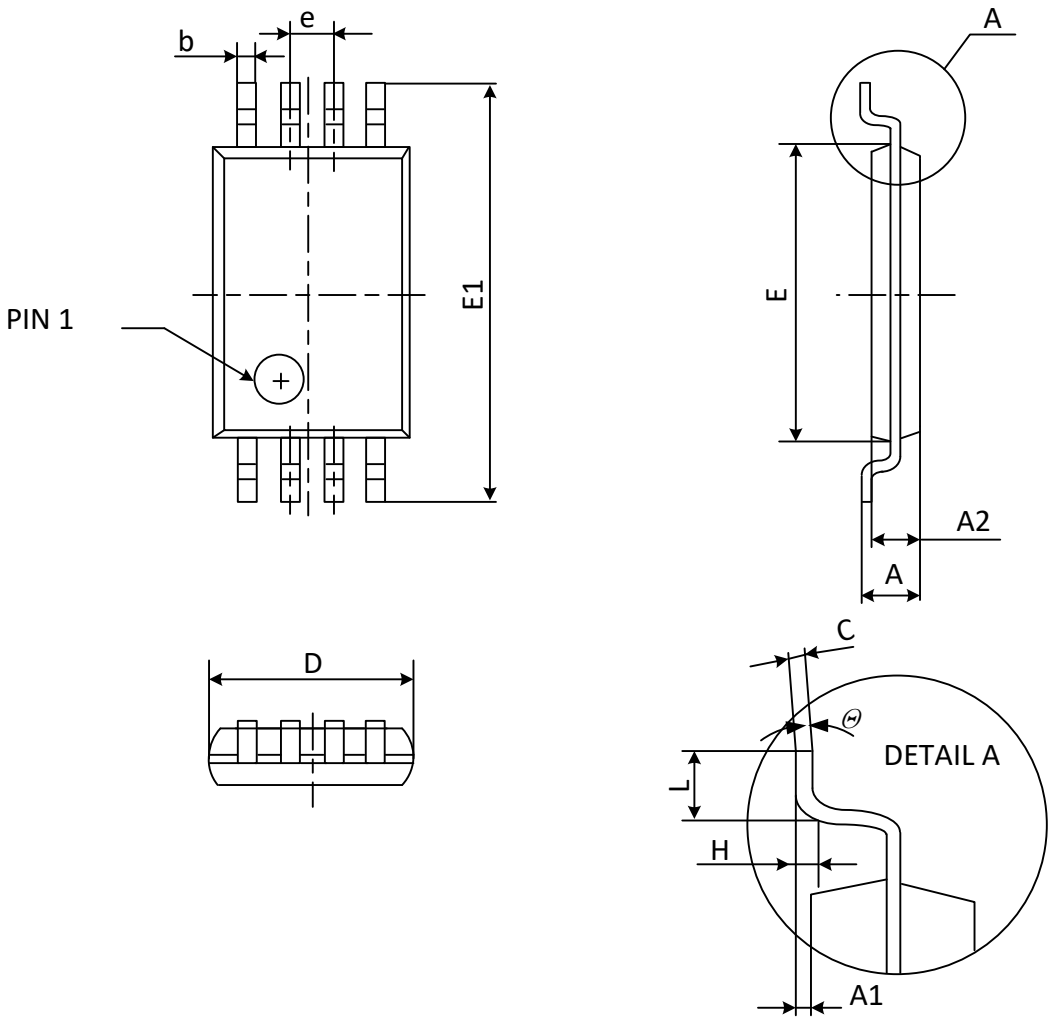


Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	1.750	1.950	2.160
A1	0.050	0.150	0.250
A2	1.700	1.800	1.910
b	0.350	0.420	0.480
c	0.190	0.20	0.250
D	5.130	5.230	5.330
E	7.700	7.900	8.100
E1	5.180	5.280	5.380
e	1.270 BSC		
L	0.500	0.650	0.800
θ	0°	----	8°

Note:

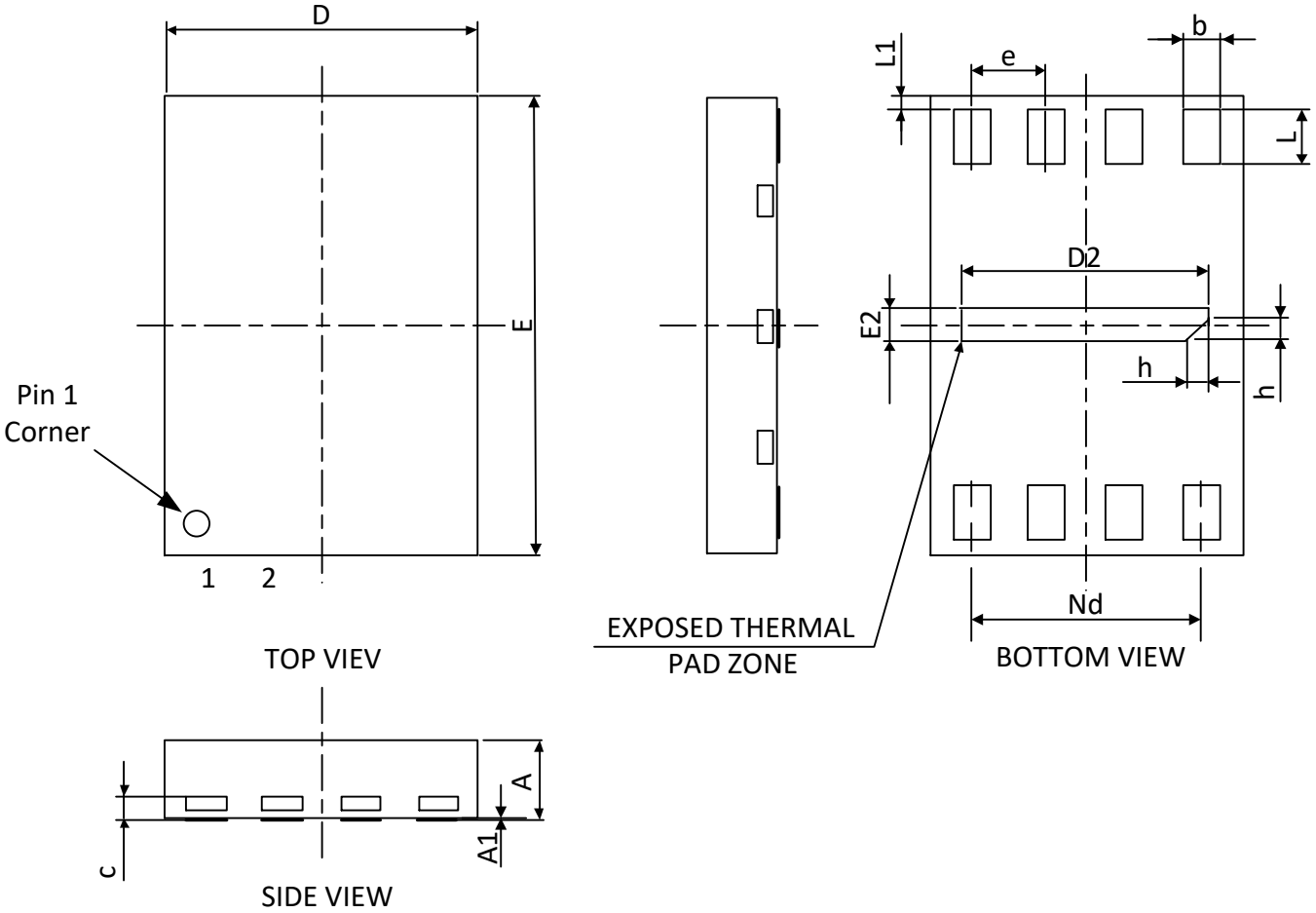
1. JEDEC Outline : N/A
2. Coplanarity: 0.1mm
3. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.

9.3. Package TSSOP8 173MIL



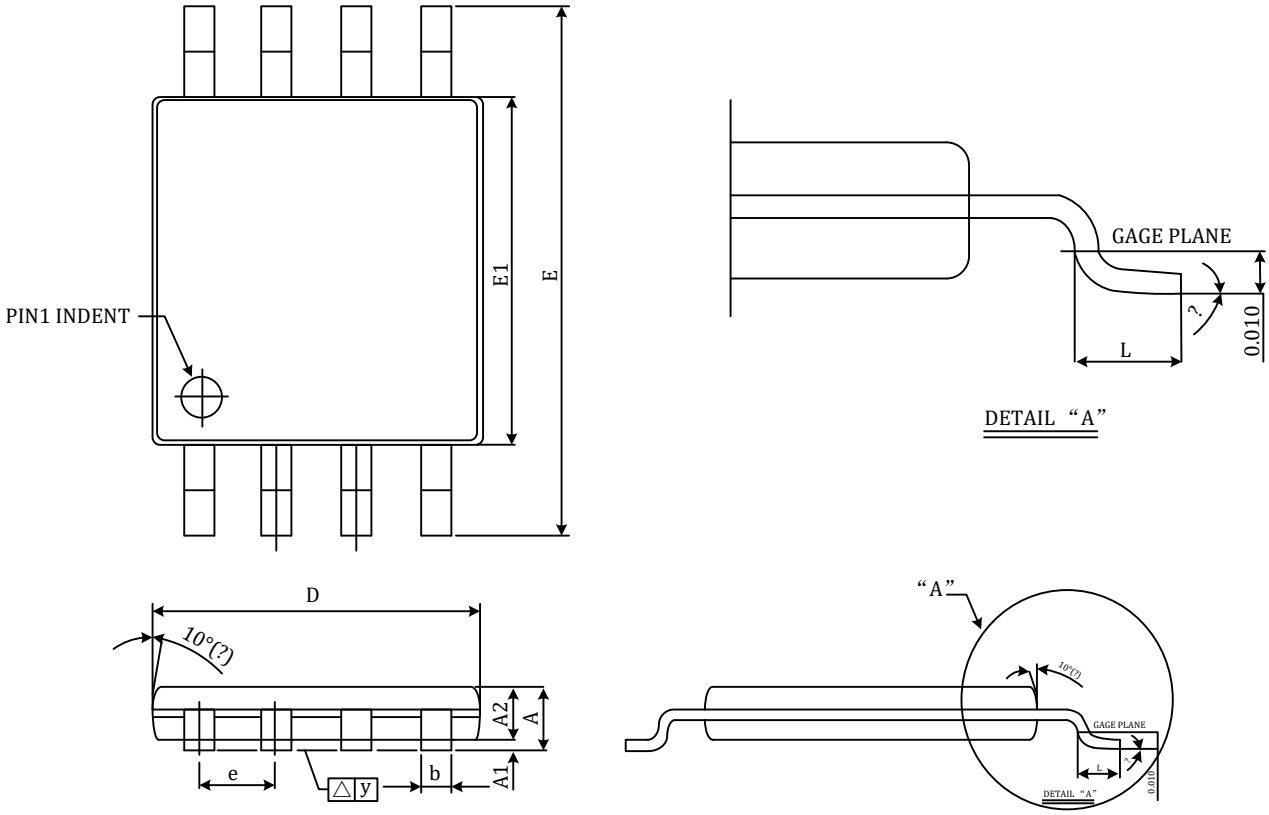
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

9.4. Package DFN8 (2x3x0.55) mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
L	0.30	0.35	0.40
L1	0.05	0.10	0.15
h	0.05	0.15	0.25

9.5. Package VSOP 208MIL



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	--	1.000	--	0.039
A1	0.050	0.150	0.002	0.006
A2	0.750	0.850	0.030	0.033
b	0.350	0.480	0.014	0.019
c	0.127 (REF)		0.005 (REF)	
D	5.180	5.380	0.204	0.212
E	7.700	8.100	0.303	0.319
E1	5.180	5.380	0.204	0.212
e	--	--	--	--
L	0.500	0.800	0.020	0.031
y	--	0.100	--	0.004
θ	0°	8°	0°	8°

10. REVISION HISTORY

Revision	Description	Date
1.0	Initial Release base 4M rev 0.7/0.5/0.6	Aug-01-2018
1.1	Correct the mistake on Single/Dual/Quad	Oct-12-2018
1.2	Revise to correct typo error for status register S4 change reserved to BP2 at page #8	Nov-12-2018
1.3	Revise to include UID support Revise to split into individual density 4M datasheet	Dec-18-2018 Dec-24-2018
1.4	Revise to correct Package DFN 2x3x0.55mm and block diagram.	Mar-22-2019
1.5	Revise to update 7.1 Power-on Timing description	Sep-17-2019