XT25F02E

Dual IO Serial NOR Flash
Datasheet

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Serial NOR Flash Memory

2M bits 3.3V Dual I/O Serial Flash Memory with 4KB Uniform Sector

- **2M -bit Serial Flash**
  - 256 K-byte
  - 256 bytes per programmable page
- **Standard, Dual SPI**
  - Standard SPI: SCLK, CS#, SI, SO
  - Dual SPI: SCLK, CS#, IO0, IO1
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 64k-byte
- **Software Write Protection**
  - Write protect all/portion of memory via soft-ware
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halo-gen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40℃ to +85℃), MSL3
- **Low Power Consumption**
  - 20mA maximum active current
  - 13uA Standby current
- **Single Power Supply Voltage: Full voltage range:**
  - 2.7~3.6V
- **Support 128 bits Unique ID**
- **Minimum 100,000 Program/Erase Cycle**
- **High Speed Clock Frequency**
  - 120MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 160Mbits/s
- **Program/Erase Speed**
  - Page Program time: 1.3ms typical
  - Sector Erase time: 75ms typical
  - Block Erase time: 0.5s typical
  - Chip Erase time: 1.7s typical

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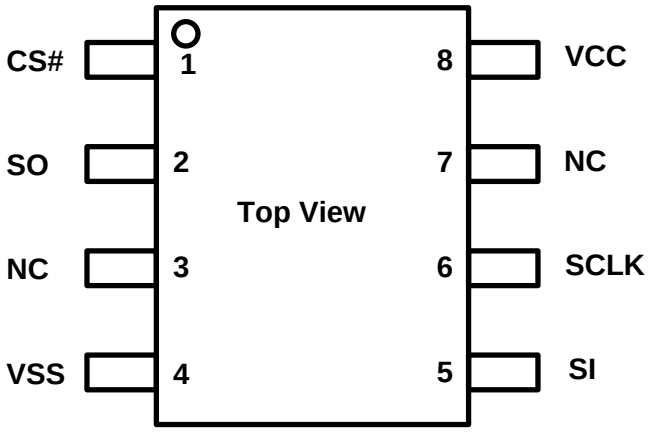
1. GENERAL DESCRIPTION

The XT25F02E Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO). The Dual I/O data is transferred at a speed of 160Mbits/s.

1.1. Available Ordering OPN

OPN	Package Type	Package Carrier
XT25F02ESOIGU	SO8 150mil	Tube
XT25F02ESOIGT	SO8 150mil	Tape & Reel
XT25F02EDTIGT	DFN8 2x3x0.40mm	Tape & Reel

1.2. Connection Diagram

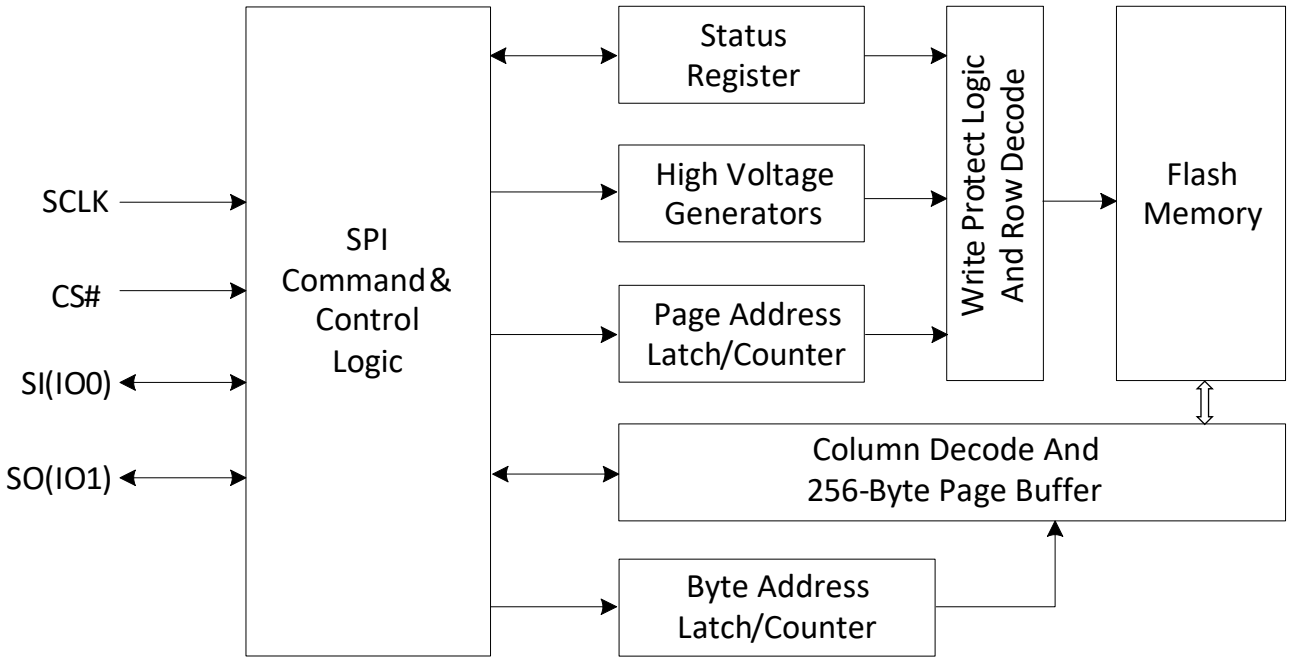


8 – LEAD SOP / DFN8

1.3. Pin Description

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
VCC		Power Supply

1.4. Block Diagram



2. MEMORY ORGANIZATION

XT25F02E Memory Description

Each Device has	Each block has	Each sector has	Each page has	
256K	64K	4K	256	bytes
1K	256	16	-	pages
64	16	-	-	sectors
4	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

XT25F02E 64K Bytes Block Sector Architecture

Block	Sector	Address range	
3	63	03F000H	03FFFFH
	……	……	……
	48	030000H	030FFFH
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

3. DEVICE OPERATION

Standard SPI

The XT25F02E features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The XT25F02E supports Dual SPI operation when using the "Dual Output Fast Read" and "Dual I/O Fast Read" (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4. DATA PROTECTION

The XT25F02E provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode:
  - Block Protect (BP1, BP0) bits define the section of the memory array that can be read and change.

Table1.0 XT25F02E Protected area size

Status bit		Protect Level	Protected Block
BP1	BP0		
0	0	0(none)	None
0	1	1(1 block)	Block 0
1	0	2(2 blocks)	Block 0-1
1	1	3(4 blocks)	Protected All

5. STATUS REGISTER

S7	S6	S5	S4	S3	S2	S1	S0
Reserved	Reserved	Reserved	Reserved	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP1, BP0 bits.

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1.0) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. Chip Erase command will be ignored if one or more of the Block Protect (BP1, BP0) bits are 1.

6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable or Write Disable command, CS# must be driven high exactly at the byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Enable for Volatile Status Register	50H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Write Status Register	01H	(S7-S0)					
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 Dummy(2)	(D7-D0)(1)			(continuous)
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
Read Unique ID	4BH	00H	00H	00H	(D7-D0)		
Enable Reset	66H						
Reset	99H						

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

Table of ID Definitions:

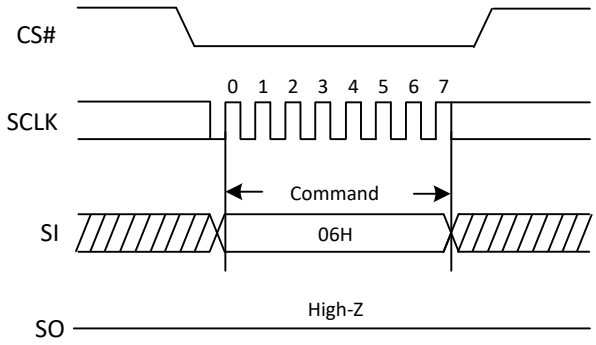
XT25F02E

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0B	40	12
90H	0B		11
ABH			11

6.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low→sending the Write Enable command→CS# goes high.

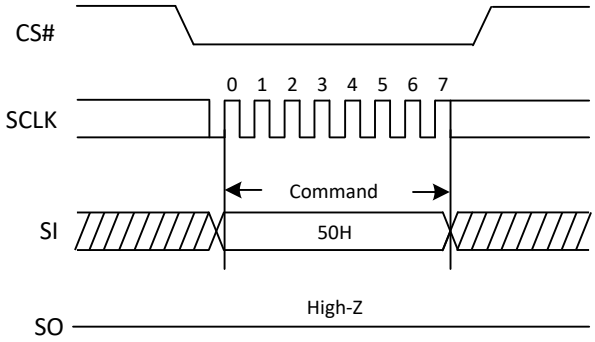
Figure1. Write Enable Sequence Diagram



6.2. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

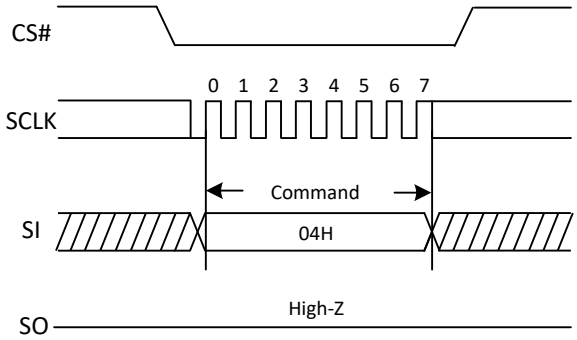
Figure2. Write Enable for Volatile Status Register Sequence Diagram



6.3. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→sending the Write Disable command→CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

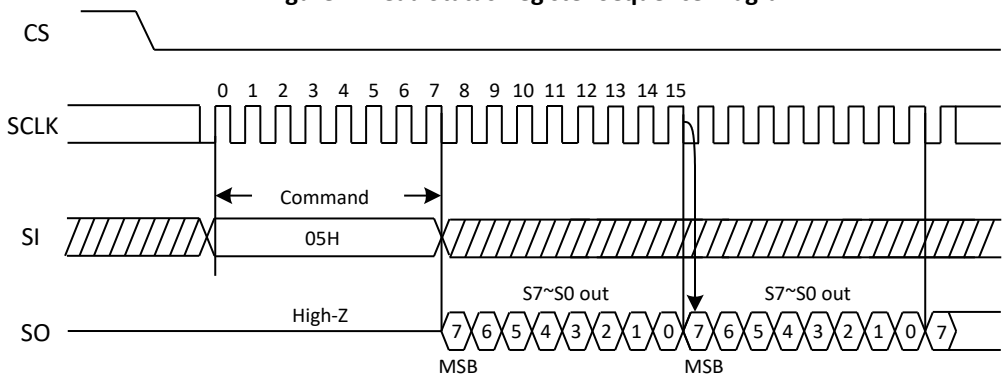
Figure 3. Write Disable Sequence Diagram



6.4. Read Status Register (RDSR) (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously.

Figure 4. Read Status Register Sequence Diagram



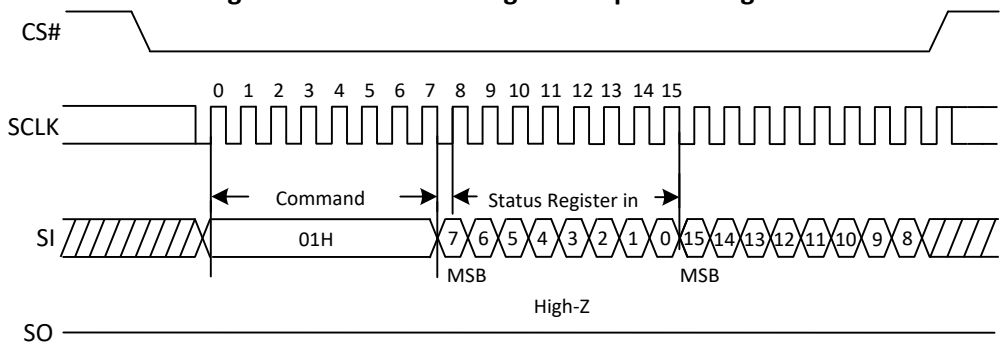
6.5. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S6, S5, S4, S1 and S0 of the Status Register. CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tw) is initiated. While the Write Status Register cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1.0.

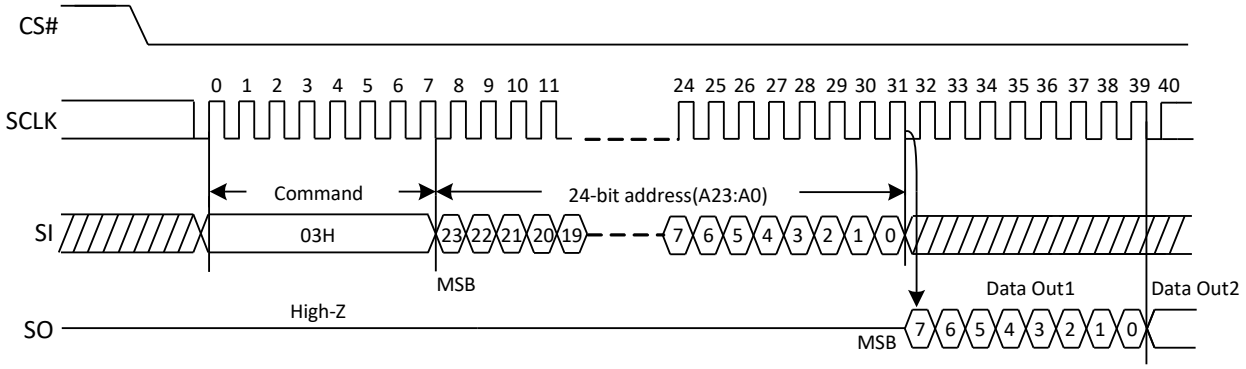
Figure 5. Write Status Register Sequence Diagram



6.6. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

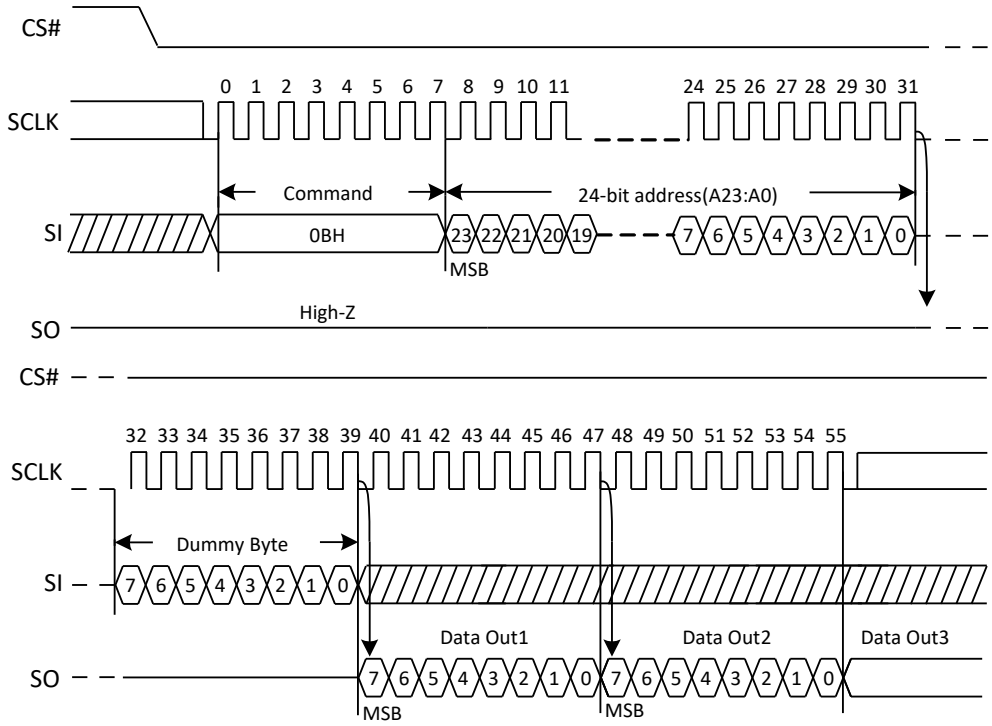
Figure 6. Read Data Bytes Sequence Diagram



6.7. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for fast reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

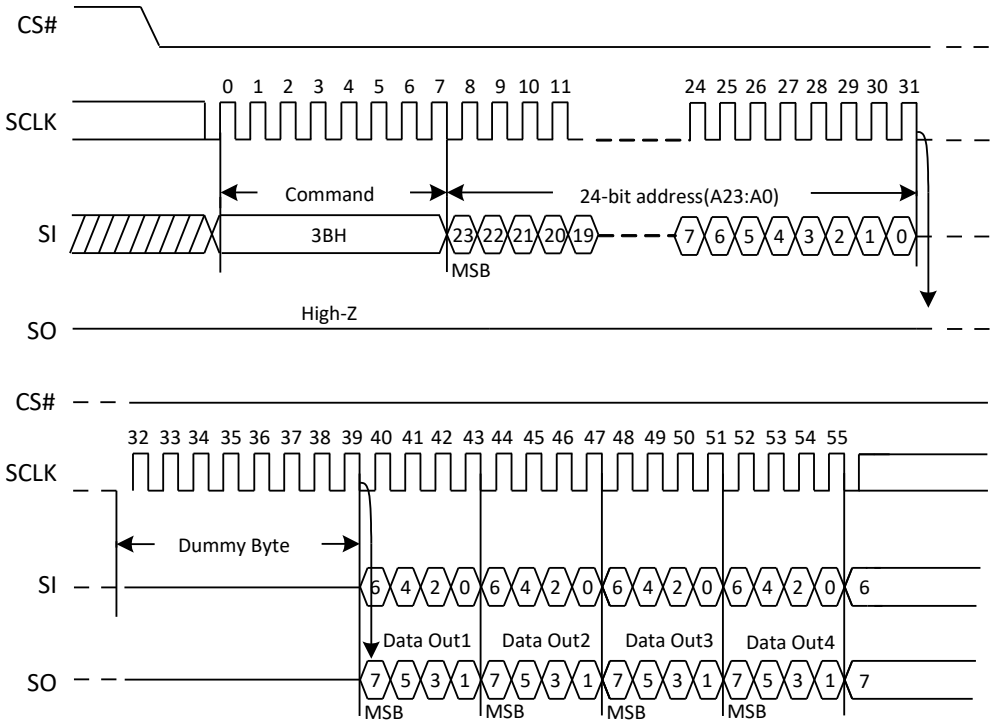
Figure 7. Read Data Bytes at Higher Speed Sequence Diagram



6.8. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

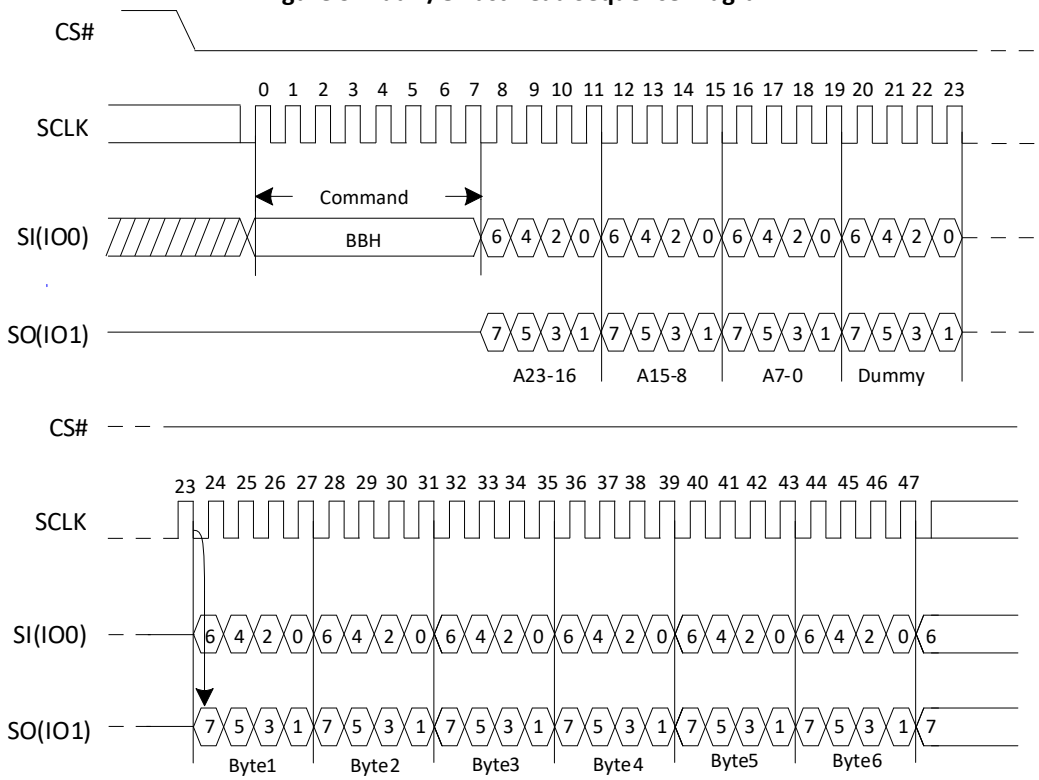
Figure 8. Dual Output Fast Read Sequence Diagram



6.9. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 9. Dual I/O Fast Read Sequence Diagram



6.10. Page Program (PP) (02H)

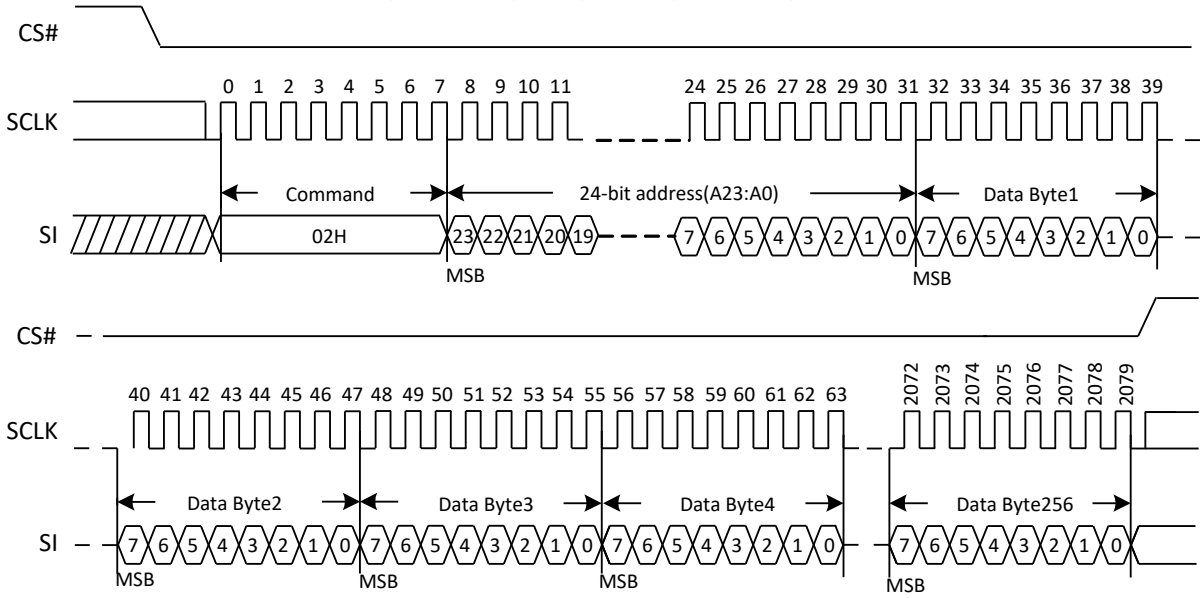
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure 10. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP1, BP0) is not executed.

Figure 10. Page Program Sequence Diagram

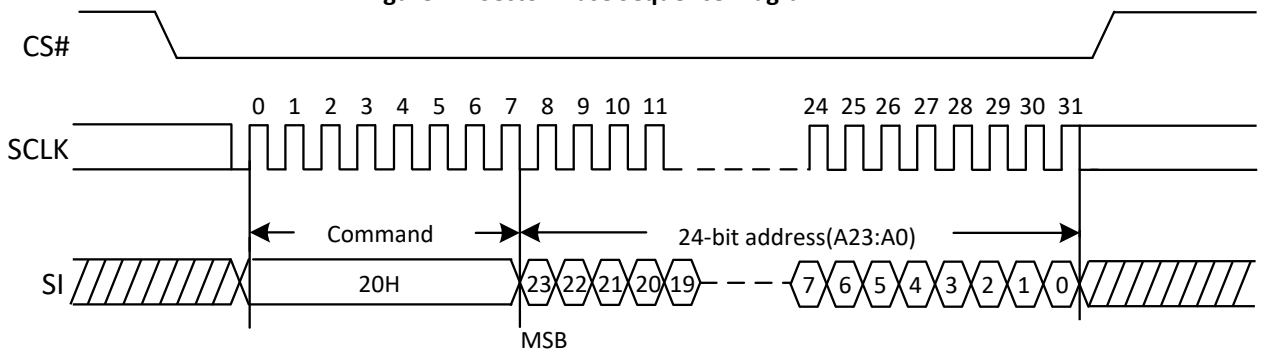


6.11. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low →sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 11. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP1, BP0) bit (see Table1.0) is not executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 11. Sector Erase Sequence Diagram

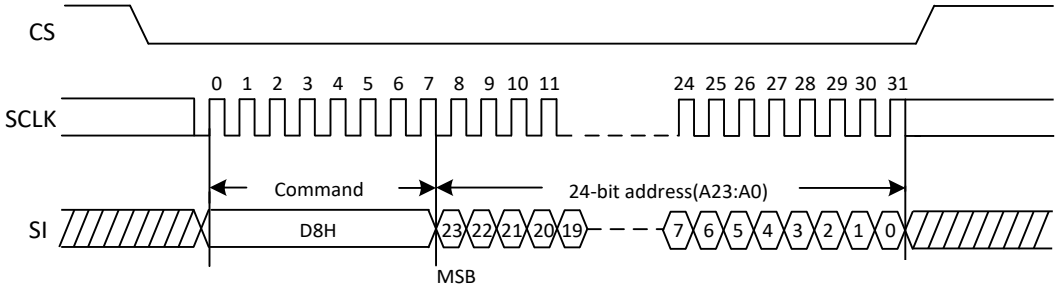


6.12. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command →3byte address on SI → CS# goes high. The command sequence is shown in Figure 12. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP1, BP0) bits (see Table1.0) is not executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 12. 64KB Block Erase Sequence Diagram

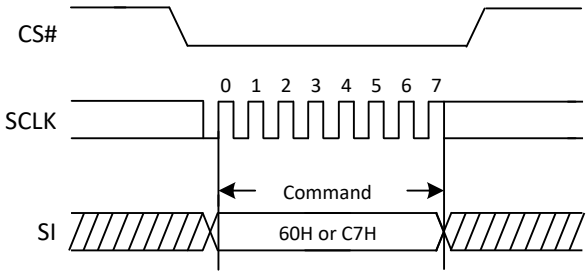


6.13. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure 13. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP1, BP0) bits are all 0. The Chip Erase (CE) command is ignored if one or more sectors are protected. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 13. Chip Erase Sequence Diagram

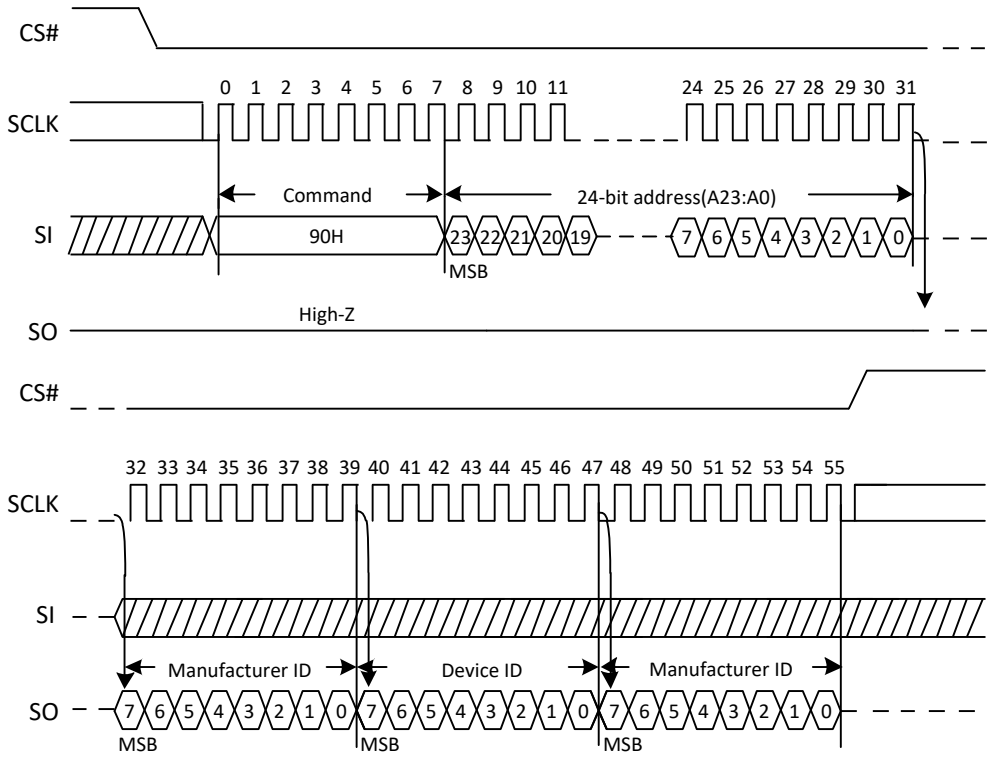


6.14. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 17. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 17. Read ID Sequence Diagram

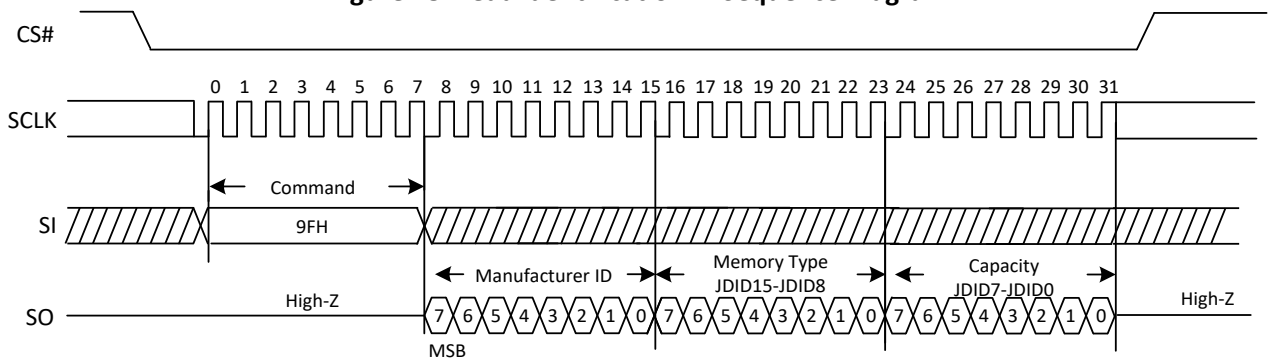


6.15. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure18. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 18. Read Identification ID Sequence Diagram



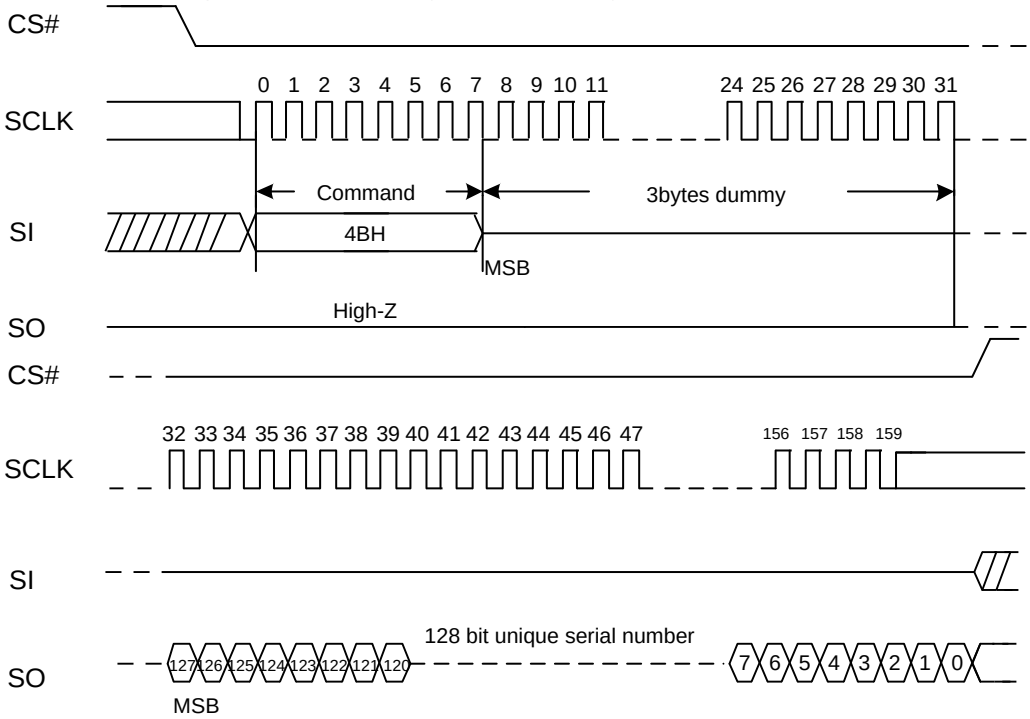
6.16. Read Unique ID (RUID) (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each XT25F02E device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →00H →00H →00H → 128bit Unique ID Out → CS# goes high.

The command sequence is show below.

Figure 18.1 Read Unique ID (RUID) Sequence (Command 4B)

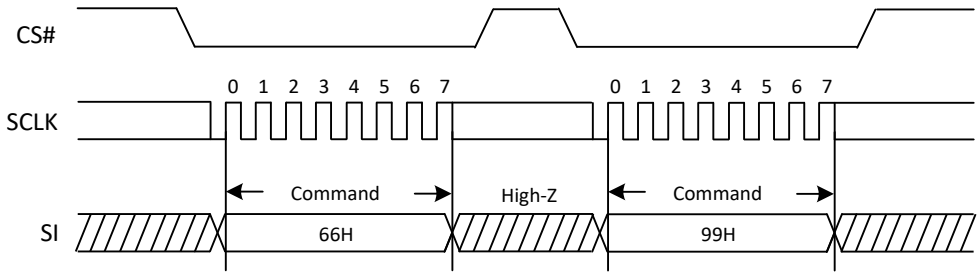


6.17. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL).

The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRSTR to reset. During this period, no command will be accepted.

Figure 19. Enable Reset and Reset command Sequence Diagram



7. ELECTRICAL CHARACTERISTICS

7.1. Power-on Timing

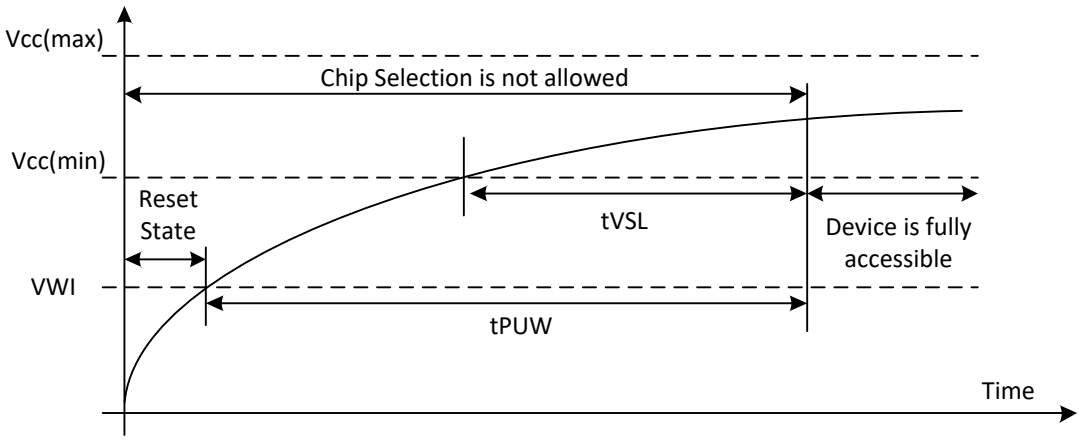


Table3. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC(min) To CS# Low	10		us
t_{PUW}	Time Delay Before Write Instruction	1	10	ms
V_{WI}	Write Inhibit Voltage	1	2.5	V

7.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

7.3. Data Retention and Endurance

Parameter	Typical	Unit
Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

7.4. Latch up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

7.5. Absolute Maximum Ratings

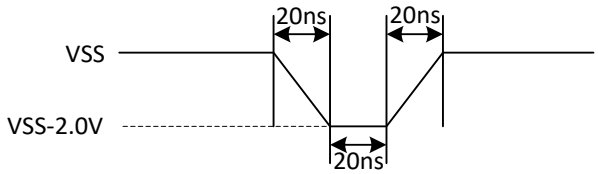
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

7.6. Capacitance Measurement Condition

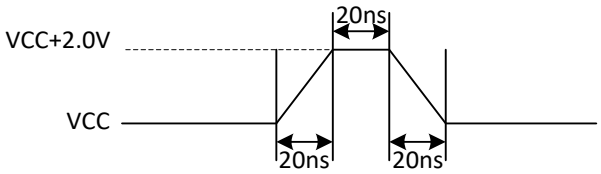
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 20. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



7.7. DC Characteristics

(T=-40℃~85℃,VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	CS#=VCC VIN=VCC or VSS		13	20	µA
I_{CC3}	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 40MHZ,Q=Open(*1 I/O)		5	6	mA
		CLK=0.1VCC/0.9VCC at 100MHZ,Q=Open(*1 I/O)		9	11	mA
I_{CC4}	Operating Current(PP)	CS#=VCC			20	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			20	mA
I_{CC6}	Operating Current(SE)	CS#=VCC			20	mA
I_{CC7}	Operating Current(BE)	CS#=VCC			20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL=1.6mA			0.4	V
V_{OH}	Output High Voltage	IOH=-100uA	VCC-0.2			V

7.8. AC Characteristics

(T=-40℃~85℃,VCC=2.7~3.6V， C_L=30pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
fC	Serial Clock Frequency For: Fast Read (0BH), Dual Output (3BH)			120	MHz
fC1	Serial Clock Frequency For: Dual I/O (BBH)			80	MHz
fR	Serial Clock Frequency For: Read (03H)			50	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time (read/write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tCLQV	Clock Low To Output Valid			6.5	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tRES1	CS# High To Standby Mode Without Electronic Signature Read			0.5	us
tRES2	CS# High To Standby Mode With Electronic Signature Read			0.5	us
tW	Write Status Register Cycle Time		70	1000	ms
tPP	Page Programming Time		1.3	3.0	ms
tSE1	Sector Erase Time (25℃~85℃)		75	1000	ms
tSE2	Sector Erase Time (-40℃~25℃)		75	2000	ms
tBE	Block Erase Time (64K Bytes)		0.5	2.0	s
tCE	Chip Erase Time (2M)		1.7	5.0	s

Figure 21. Serial Input Timing

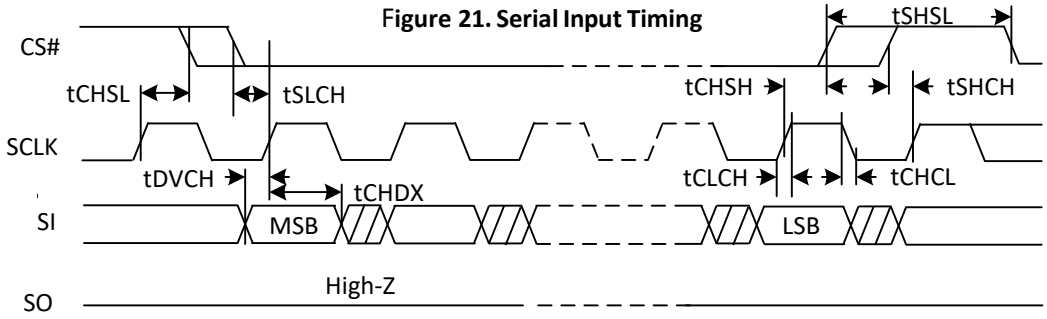
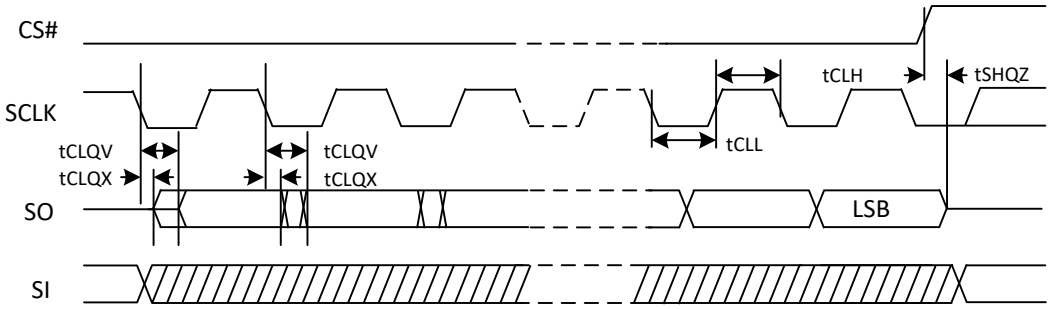


Figure 22. Output Timing



Least significant address bit (LSB) in

8. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following

XT 25F 02E SO I G U

Company Prefix

XT = XTX

Product Family

25F = 2.7~3.6V Serial Flash Memory
with 4KB Uniform-Sector

Product Density

02E = 2M bit

Product Package

SO = 8-pin SOP8(150mil)
DT = 8-pad DFN8(2x3x0.40mm)

Temperature & Moisture Sensitivity Level

I = Industrial Level Temp. (-40℃ to +85℃), MSL3

Green Code

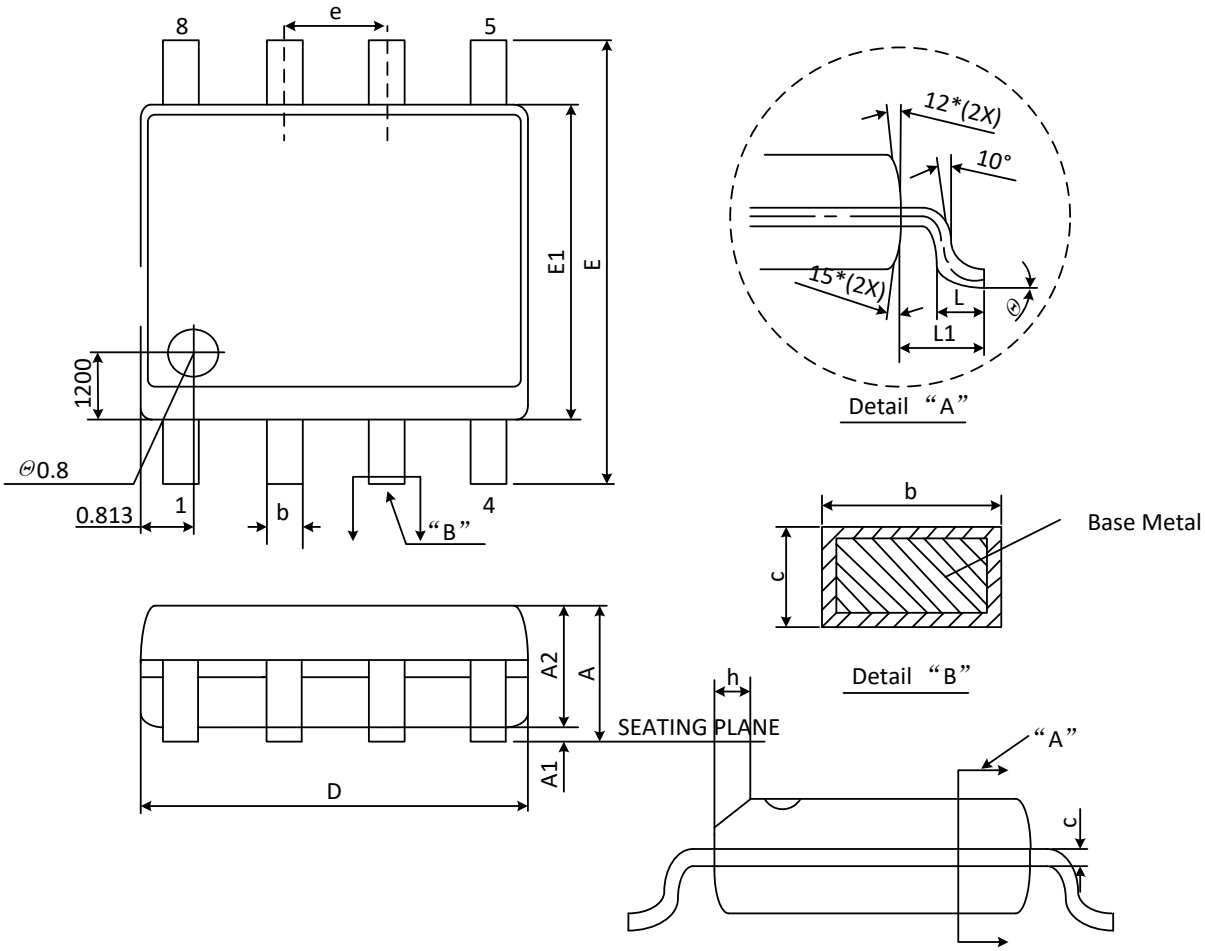
G = Green/Reach Package

Product Carrier

U = Tube; **T** = Tape & Reel; **A** = Tray

9. PACKAGE INFORMATION

9.1. Package SOP8 150MIL

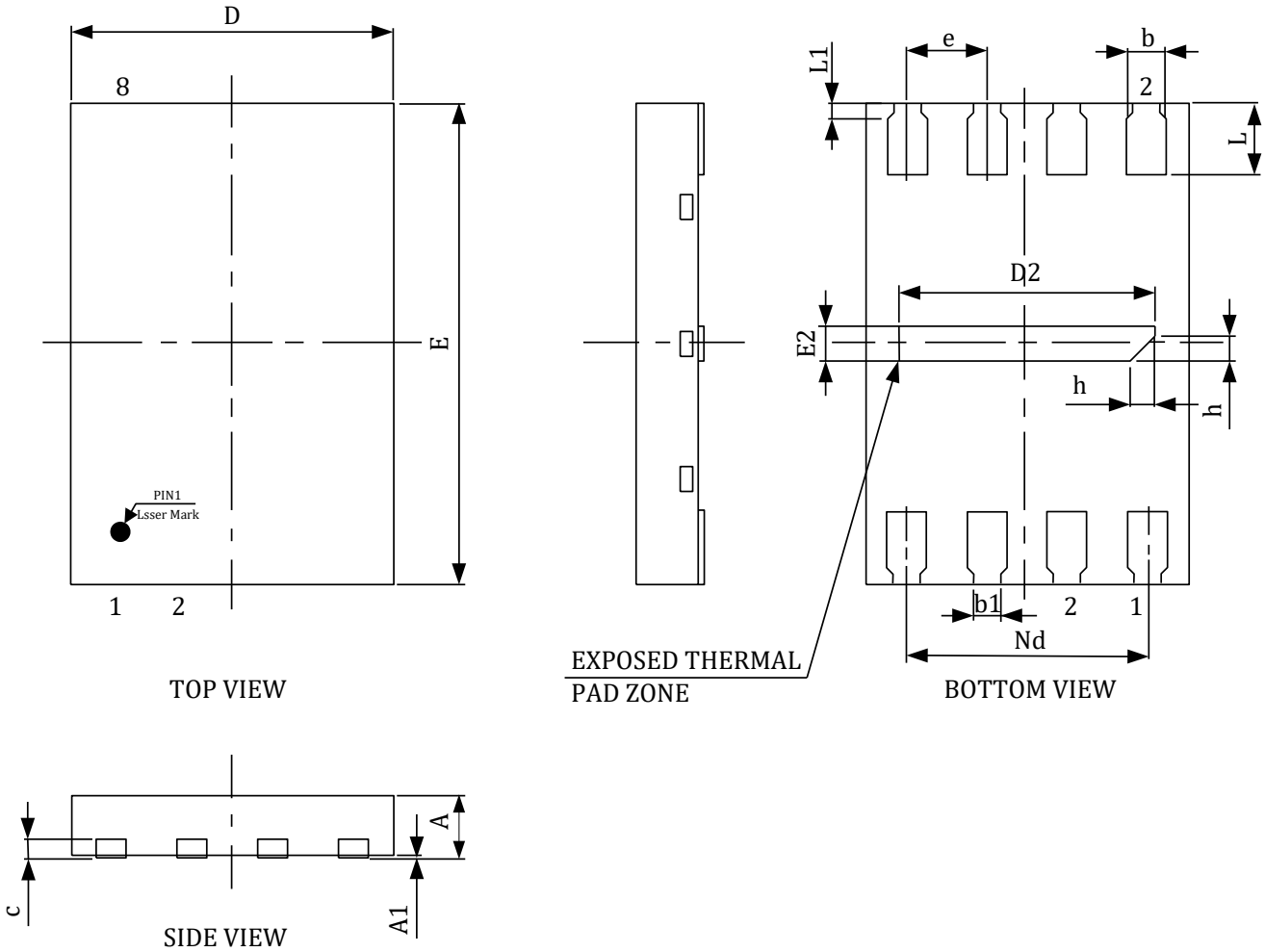


Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	1.350	----	1.750
A1	0.100	----	0.250
A2	1.300	----	1.500
b	0.330	----	0.510
c	0.190	----	0.250
D	4.700	4.900	5.000
E1	3.800	3.900	4.000
e	----	1.270	----
E	5.800	6.000	6.200
h	0.2500	0.350	0.500
L	0.508	0.635	0.762
L1	0.837	1.040	1.243
θ	0°	----	8°

Note:

1. Coplanarity: 0.1mm
2. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.
3. All dimensions follow JEDEC MS-012 standard.

9.2. Package DFN8 (2x3x0.40) mm



Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	0.36	--	0.40
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.127REF		
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e	0.50 BSC		
Nd	1.50 BSC		
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
L	0.40	0.45	0.50
L1	0.05	0.10	0.15
h	0.05	0.15	0.25

10. REVISION HISTORY

Revision	Description	Date
1.0	Initial version based on XT25F02E-B	Nov-25-2019
1.1	Corrected mistake of page size in memory description and feature.	April 1, 2020