MK SPI NAND Product Datasheet
Industrial Grade

Product List

MKSV1GIL-AE
MKSV2GIL-AE

Revision History

Version	Date	Description
Rev 1.0	*2024/06/10*	*Released*

Notice :

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1 FEATURE

- 1/2Gb SLC NAND Flash

- Flash Size
  - Page size: (2048+128) byte,
  - Block size: (128K+8K) byte

- Standard, Dual, Quad SPI
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, SIO0, SIO1,WP#, HOLD#
  - Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
  - 3.3V: 104MHz for fast read with 30pF load
  - 3.3V: Quad I/O Data transfer up to 416Mbits/s
  - 3.3V: Quad I/O Data transfer up to 416Mbits/s

- characteristics
  - ECC Correction
  - Bad blockmanagement
  - Wear Leveling
  - Power loss protection

- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Register protection with WP# Pin

- Single Power Supply Voltage
  - Full voltage range for 3.3V: 2.7V~ 3.6V

- Advanced security Features
  - 8 page ,32K-Byte OTP Region

- Program/Erase/Read Speed
  - Page Program time: 600us typical
  - Cache Program time: 20us minimum
  - Block Erase time: 3ms maximum
  - Random page read time: 280us typical
  - Sequence page read/Cache read time: 20us minimum

- Low Power Consumption
  - 30mA max erase/program current
  - 28mA max read current
  - 65uA typical standby current

- Enhanced access performance
  - 2Kbyte cache for fast random read
  - Cache read and cache program

- Advanced Feature for NAND
  - Factory good block0

- Reliability
  - P/E cycles with ECC: 100K
  - Data retention: 10Years

- Internal ECC
  - 8bits /512Byte

Note: (1). ECC is on default, which can be disable by user.

2 GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra-cost effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI and standard parallel NAND Flash, with advanced features:

- Total pin count is 8, including VCC and GND
- Superior write performance and cost per bit over SPI
- Significant low cost than parallel NAND

This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pin out from one density to another. The command sets resemble common SPI command sets, modified to handle NAND specific functions and added new features. SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

- **User-selectable internal ECC**. ECC parity is generated internally during a page program operation. When a page is read to the cache register, the ECC parity is detected and corrects the errors when necessary. The device outputs corrected data and returns an ECC error status.
- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data. This command string can only be used on blocks with the same parity attribute.
- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correct by internal ECC when ECC enabled.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

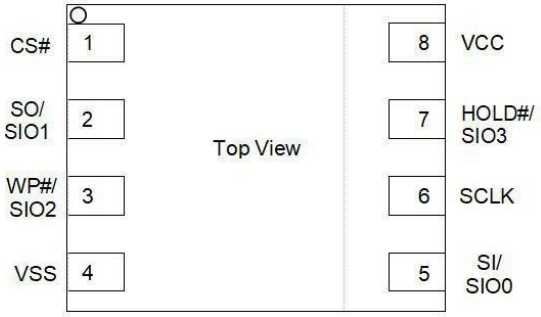
2.1 Product List

Please contact regional sales for the latest product selection and available form factors

Product Number	Density	Voltage	Package Type	ECC
MKSV1GIL-AE	1G bit	2.7~3.3V	LGA8 6.0*8.0mm	8bit/512
MKSV2GIL-AE	2G bit	2.7~3.3V	LGA8 6.0*8.0mm	8bit/512

2.2 CONNECTION DIAGRAM

Figure 2-1.Connect Diagram



2.3 PIN DESCRIPTION

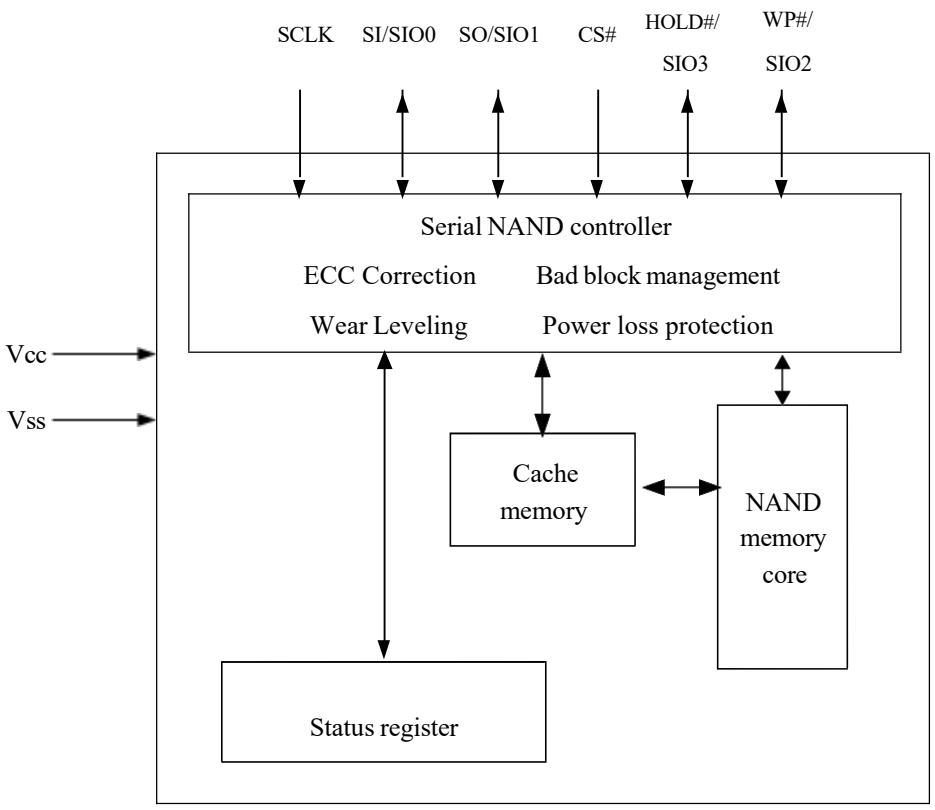
Pin Name	I/O	Description
CS#	I	Chip Select input, active low
SO/SIO1	I/O	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	I/O	Write Protect, active low / Serial Data Input Output 2
VSS	Ground	Ground
SI/SIO0	I/O	Serial Data Input / Serial Data Input Output 0
SCLK	I	Serial Clock input
HOLD# /SIO3	I/O	Hold Input, active low/Serial Data Input Output 3
VCC	Supply	Power Supply
NC		Not Connect, Not internal connection; can be driven or floated.

Note：

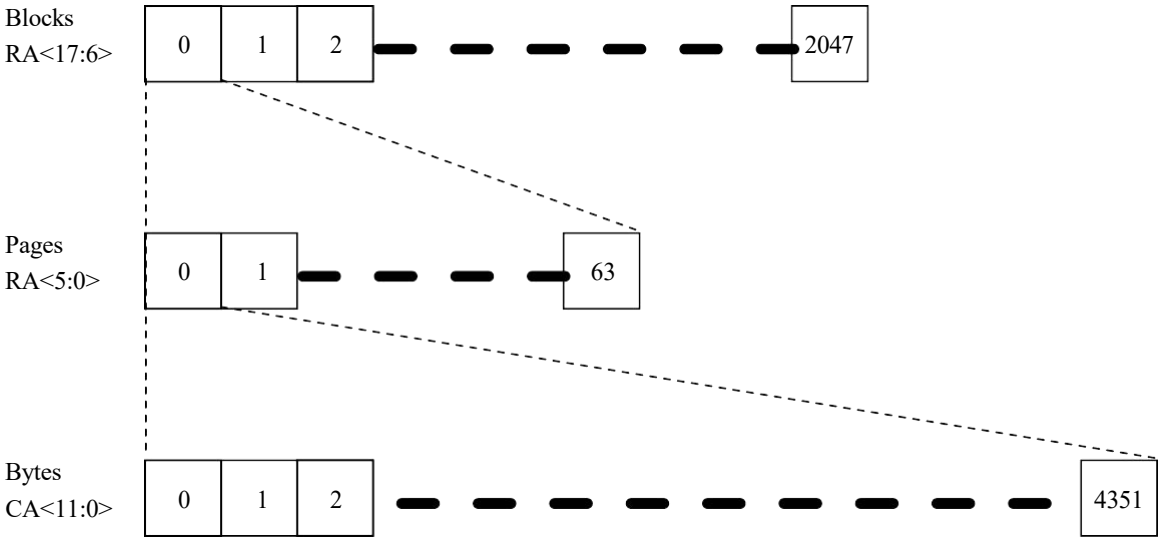
1. CS# must be driven high if chip is not selected. Please don‘t leave CS# floating any time after power is on.

2.4 BLOCK DIAGRAM

Figure 2-2.Block Diagram



3 MEMORY MAPPING



Note:

1. CA: Column Address. The 13-bit address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4352 are valid. Bytes 4224/4352 through 8191 of each page are —out of bounds,‖ do not exist in the device and cannot be addressed. CA[15:14] must be ‗0‘
2. RA: Row Address. RA<5:0>selects a page inside a block, and RA<17:6>selects a block

4 ARRAY ORGANIZATION

Table 4-1.Array Organization

MKSVXGIL-MAA			
Each device has	**Each block has**	**Each page has**	**Unit**
xGb			
1024/2048 block	128K+8K	2K+128	Bytes

5 DEVICE OPERATION

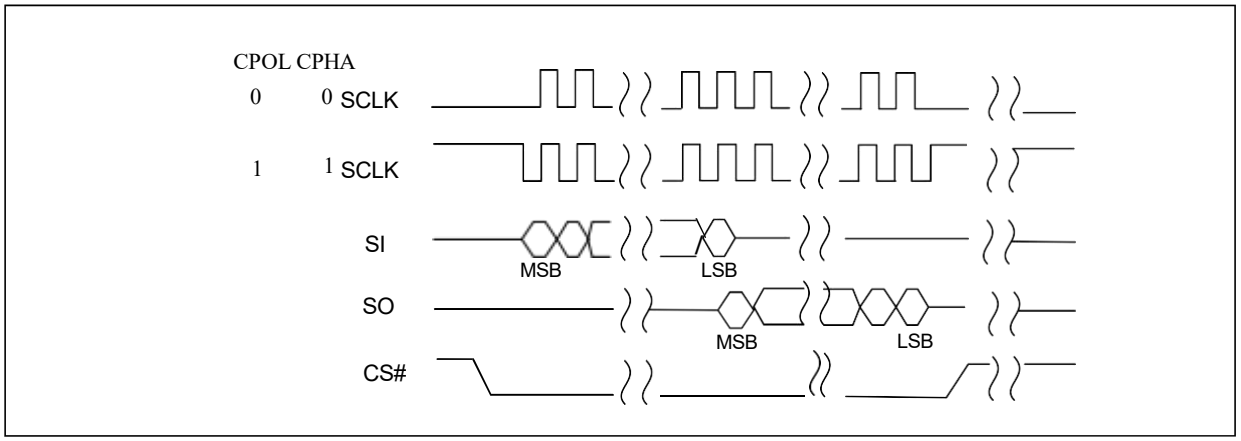
5.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. All timing diagrams shown in this data sheet are mode 0. See Figure5-1 for more details.

Figure 5-1.SPI Modes Timing Diagram



Note: While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3). Do not toggle SCLK until CS# is driven LOW.

We recommend that the user pull CS# to high when user don't use SPI flash, otherwise the flash is always in the read state, which is not good for flash.

When CS# is high and SCLK at VCC or GND state, the device is in idle state.

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

5.2 HOLD Mode

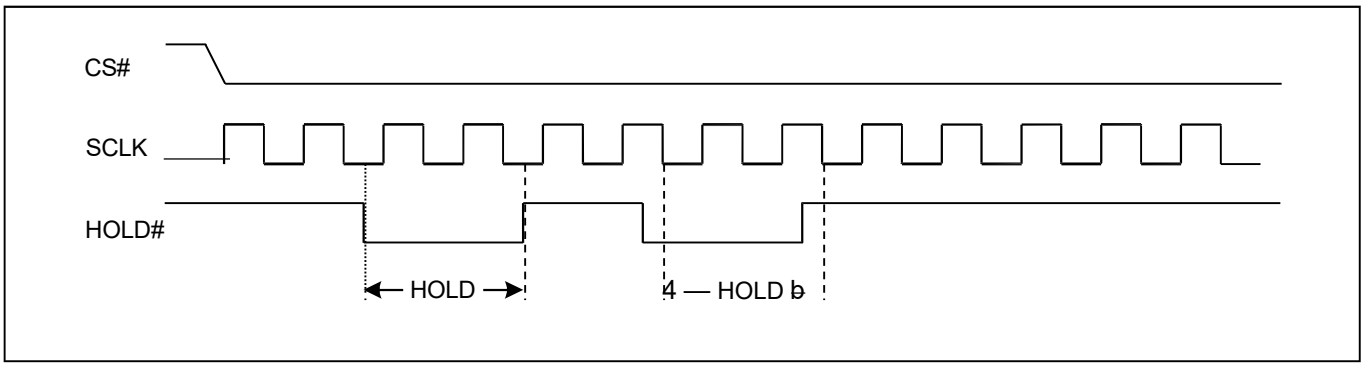
The HOLD# function is only available when QE=0 . If QE=1, the HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn‘t stop the operation of reading, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don‘t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure 5-2.Hold Condition



5.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot bealtered.

To enable the Write Protection, the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

5.4 Power Off Timing

Please do not turn off the power before Write/Erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before Write/Erase operation is complete will cause loss of data and/or damage to data.

6 COMMANDS DESCRIPTION

Table 6-1.Commands Set

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Get Features	0FH	A7-A0	D7-D0	Wrap(7)					
Set Feature	1FH	A7-A0	D7-D0						
Read ID(4)	9FH	Dummy	MID	DID1	DID2				
Page Read (to cache)	13H	PA23-16	PA15-8	P7-0	Next byte				
Page Cache Read random	30H	PA23-16	PA15-8	P7-0	Next byte				
Page Cache Read sequential	31H								
Last Page Read (to cache)	3FH								
Read From Cache	03H/0BH	CA15-8	CA7-0	Dummy	D7-D0	Next byte			
Read From Cache with 4-Byte Address	0CH	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-D0	Next byte	
Read From Cache x 2	3BH	CA15-8	CA7-0	Dummy	D7-D0 /2	Next byte			
Read From Cache x 2 with 4-Byte Address	3CH	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-D0 /2	Next byte	
Read From Cache x 4	6BH	CA15-8	CA7-0	Dummy	D7-D0 /4	Next byte			
Read From Cache x 4 with 4-Byte Address	6CH	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-0 /4	Next byte	
Read From Cache Dual IO	BBH	CA15-8 /2	CA7-0 /2	Dummy /2	D7-D0 /2	Next byte			
Read From Cache Dual IO with 4-Byte Address	BCH	CA15-8 /2	CA7-0 /2	Dummy /2	Dummy /2	Dummy /2	D7-D0 /2	Next byte	
Read From Cache Quad IO	EBH	CA15-8 /4	CA7-0 /4	Dummy /4	Dummy /4	D7-0 /4	Next byte		
Read From Cache Quad IO with 4-Byte Address	ECH	CA15-8 /4	CA7-0 /4	Dummy /4	Dummy /4	Dummy /4	Dummy /4	Dummy /4	D7-0 /4
Program Load	02H	CA15-8	CA7-0	D7-D0	Next byte				
Program Load x4	32H	CA15-8	CA7-0	D7-D0 /4	Next byte				
Program Execute	10H	PA23-16	PA15-8	PA7-0					
Program Execute background random	15H	PA23-16	PA15-8	PA7-0					
Program Load Random Data	84H	CA15-8	CA7-0	D7-D0	Next byte				
Program Load Random Data x4	C4H/34H	CA15-8	CA7-0	D7-0 /4	Next byte				

Program Load Random Data Quad IO	72H	CA15-8 /4	CA7-0 /4	D7-0 /4	Next byte				
Block Erase	D8H	PA23-16	PA15-8	PA7-0					
Reset	FFH								
Enable Power on Reset + Power on Reset	66H+99H								
Enter Deep Power-down mode	B9H								
Release Deep Power-down mode	ABH								
Bad Block Management (BBM)	A1H	LBA	LBA	PBA	PBA				
Read BBM LUT	A5H	Dummy	LBA0	LBA0	PBA0	PBA0	LBA1		
Last ECC failure Page Address	A9H	Dummy	Dummy	A15-A8	A7-A0				

7 WRITE OPERATIONS

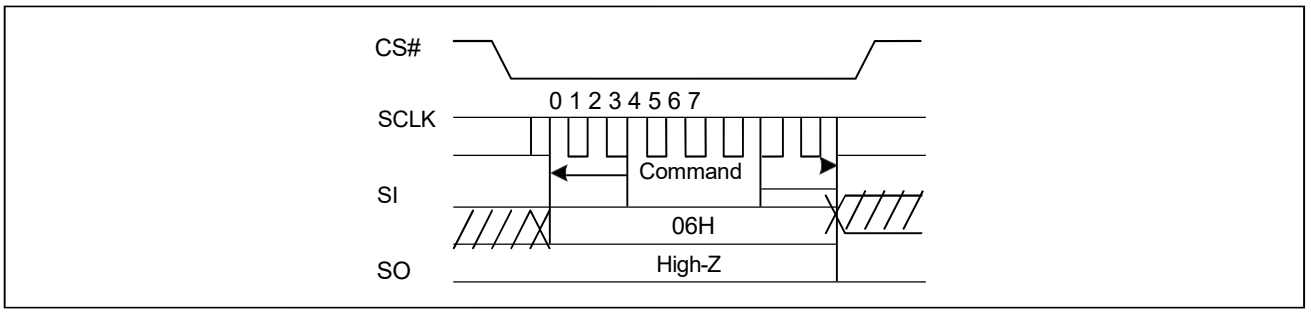
7.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Figure 7-1.Write Enable Timing Diagram

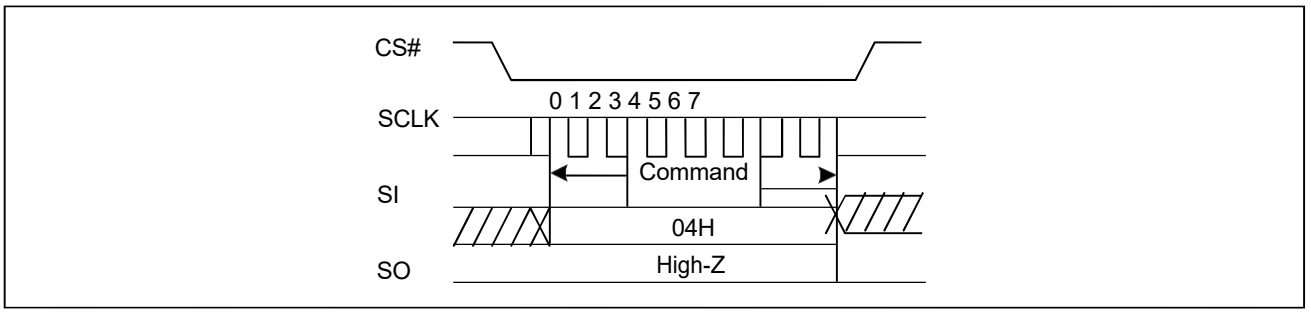


7.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Figure 7-2.Write Disable Timing Diagram



8 READ OPERATIONS

8.1 Page Read

The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13H (PAGE READ to cache)
- 0FH (GET FEATURES command to read the status)
- Read from cache command to outputdata

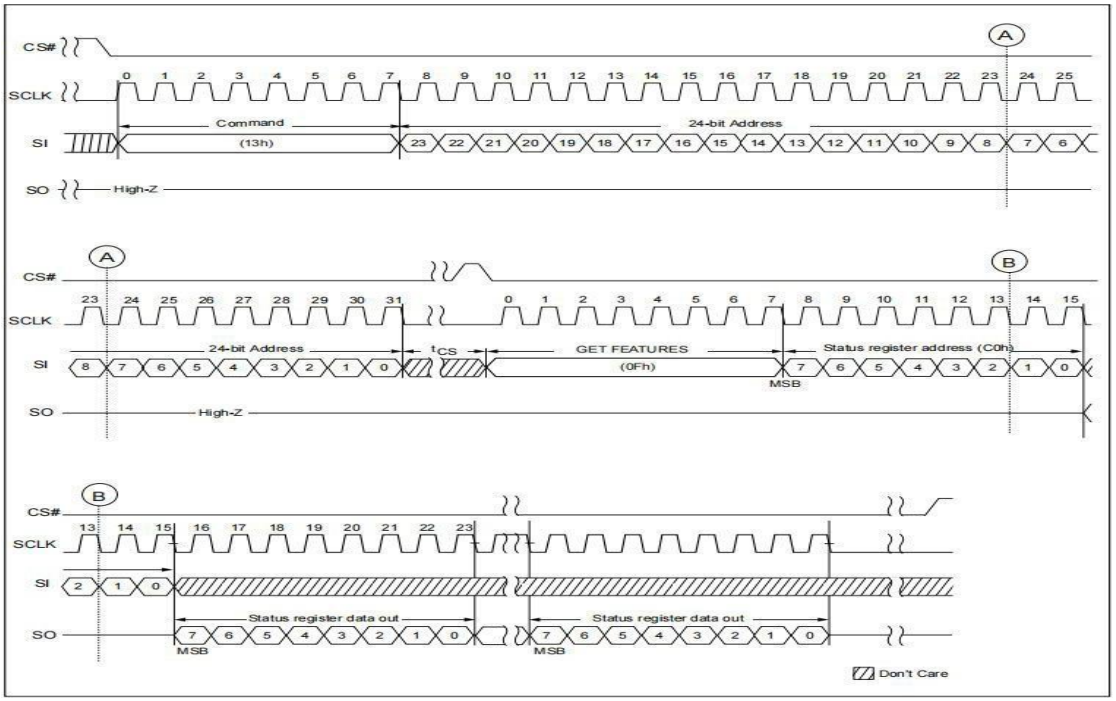
The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the GET FEATURE (0FH) command can be issued to monitor the status. Followed the page read operation, the Read From Cache command must be issued in order to read out the data from cache. The output data starts at the initial address specified in the command, once it reaches the ending boundary of whole page section, the output will return FFH until CS# is pulled high to terminate this operation. Refer waveforms to view the entire READ operation.

Note:(1) The command x4/Quad IO is only available with the QE enable.

8.2 Page Read to Cache (13H)

The command page read to cache is read the data from flash array to cache register.

Figure 8-1.Page Read Timing Diagram



8.3 Cache Read Function (30H/31H/3FH)

A ―Cache Read‖ function has been implemented in SPI series to improve the overall read throughput. It is possible to transfer the data from array to the Data Register simultaneously while a Read Data command is being performed to read out data from the Cache Register.

When multiple pages of data is to be read out sequentially, the host should issue a ―Page Read to Cache (13h)‖ command followed by a Page Address which specifies the starting page of the data(1). Once the command is accepted, the host should use ―Get Feature (0Fh)‖ to check the OIP bit value to determine if the internal operation has completed or not.

Prior to issuing a Read Data command (i.e. 03h/0Bh/3Bh/6Bh/BBh/EBh) to read out the data in the Cache Register, the host can issue a ―Page Cache Read Sequential (31h) / Page Cache Read Random (30h)‖ command to initiate the Cache Read operation. After the ―Page Cache Read Sequential (31h) / Page Cache Read Random (30h)‖ command issued, the device starts to transfer data from data register to cache register for tCBSYR. After tCBSYR, CBSY bit (through GET FEATURE command to check this status bit) goes from 1 to 0.

While the device is transferring the next page array data to the Data Register, the host can now use Read From Cache command to shift out the current page data inside the Cache Register. Once CBSY bit becomes 0, the host can issue a Read Data command to shift out the Cache Register data, then issue ―Page Cache Read Sequential (31h) / Page Cache Read Random (30h)‖ again to read the next page or special page in the array.

If the current page address is the last page of a block or the last page of the data being read out, the host should issue ―Last Page Cache Read (3Fh)‖, and proceed with the last Read from cache command. If the data being readout is more than one block, another ―Page Read to Cache (13h)‖ command is needed to specify the first page of the next block and initiate the ―Cache Read‖ operation again in the next block.

Table 8-1.Cache Read instruction description

Instruction	Command Code	Description
Page Cache Read Sequential	13h+addr+31h	Issue prior to current page ―Read From Cache‖ and read next page data into Data Register.
Page Cache Read Random	13h+addr+30h+addr	Issue prior to current page ―Read From Cache‖ and read specialize page data into Data Register.
Last Page Cache Read	3Fh	Issue prior to last page ―Read From Cache‖ at the end of a block or the end of the data being read.

Notes:

1. Upon powered up, SPI NAND will automatically load Block-0/Page-0 data into the Cache Register. If this is the starting page of the data that is to be read out, it is not necessary to issue a ―Page Read to Cache (13h)‖ command to initiate the ―Cache Read‖ operation.
2. Before issuing 30 h/ 31h/3Fh, CBSY bit must be checked to make sure CBSY=0, device is not performing any internal operations.

The command sequence is as follows:

1. 13h – PAGE READ to cache
2. 0Fh – GET FEATURE command to the read status until OIP status bit is changed from 1 to 0
3. 30h/31H – READ PAGE CACHE RANDOM/SEQUENTIAL command to transfer data from data register to cache register and kick off the next page transfer from array to data register
4. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0

5. 03h, 0Bh, 3Bh, 6Bh, BBh ……– READ FROM CACHE to read out data from cache register.

6. 0Fh – GET FEATURE command to read the status until CRBSY = 0

7. Repeat step 3 to step 6 to read out all expected pages until last page

8. 3Fh – READ PAGE CACHE LAST command to end the read page cache sequence and copy a last page from the data register to the cache register

9. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0

10. 03h, 0Bh, 3Bh, 6Bh, BBh ……– READ FROM CACHE to read out data from cache register.

Figure 8-2. Read Page Cache Random Timing

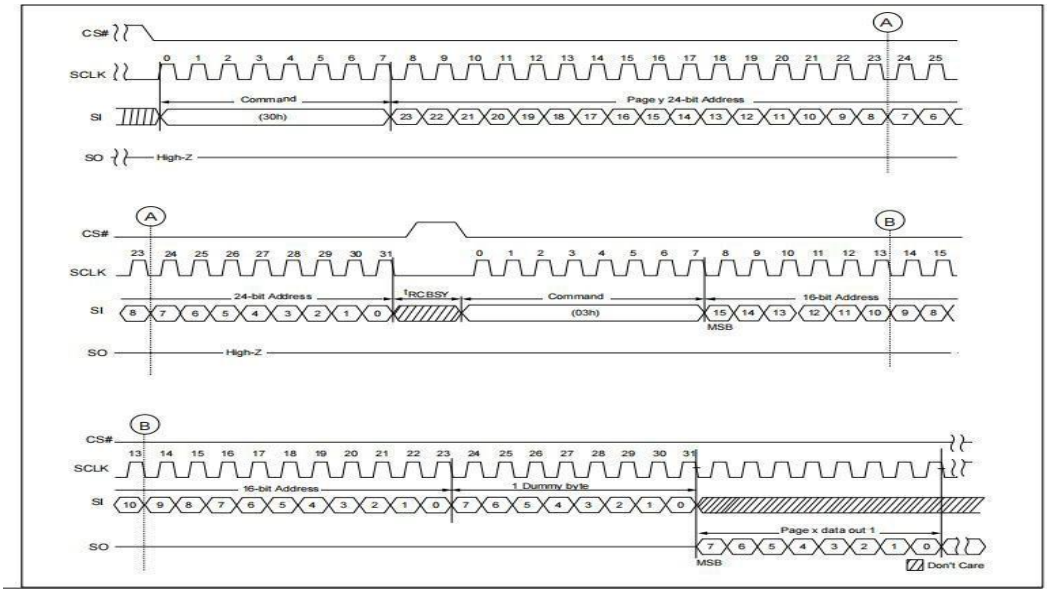


Figure 8-3. Read Page Cache Sequential Timing

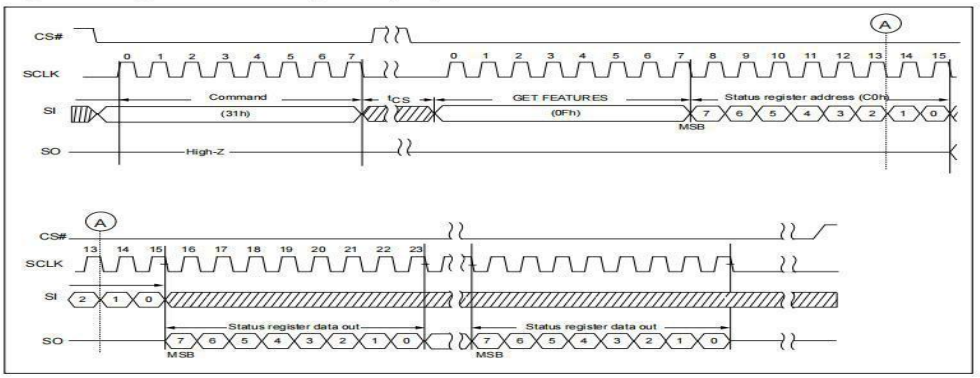


Figure 8-4. Read Page Cache Last Timing

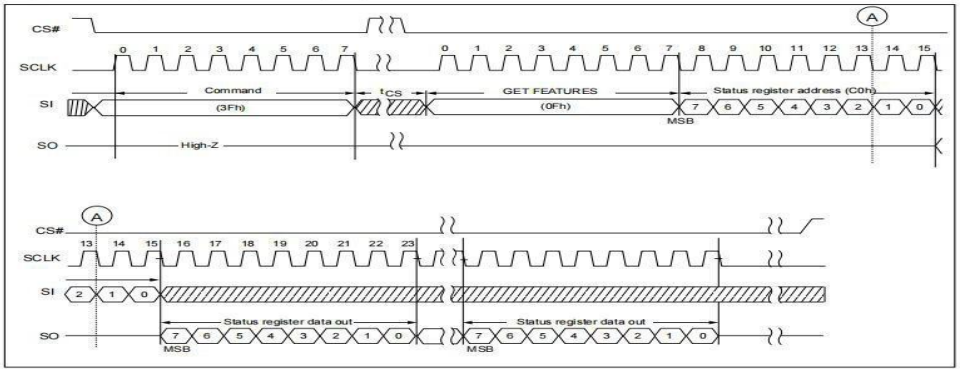
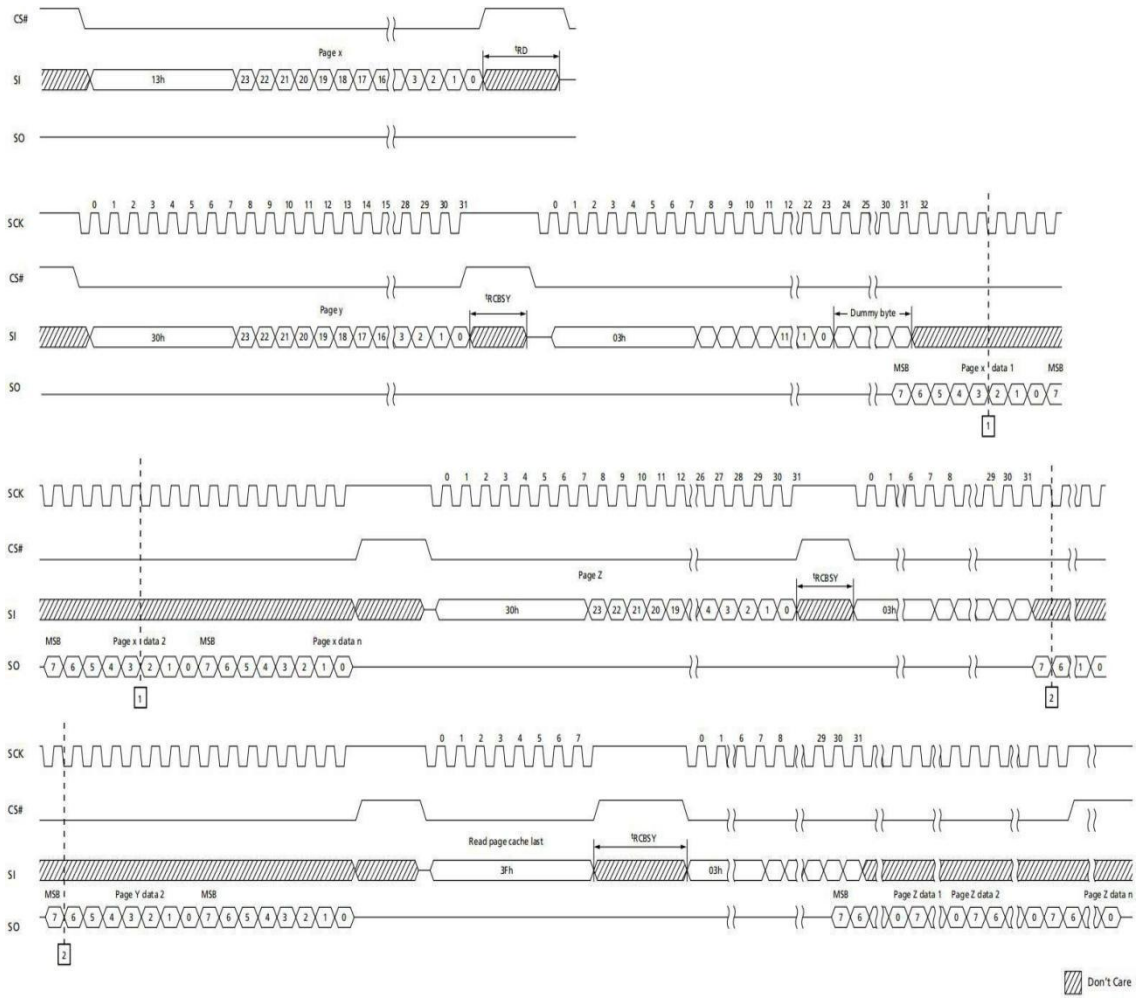


Figure 8-5. Read Page Cache Cycle Timing



Note：

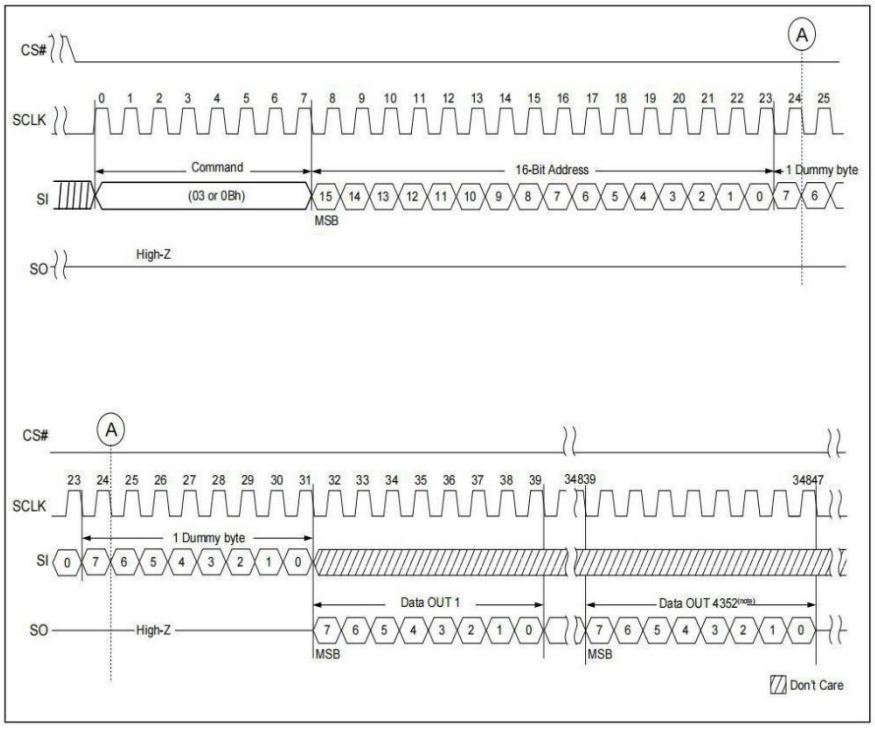
1 We recommend to use GET FEATURES command (0Fh) to read the status until CBSY=0 rather than wait busy time tRCBSY

.

8.4 Read From Cache (03H or 0BH)

The command sequence is shown below.

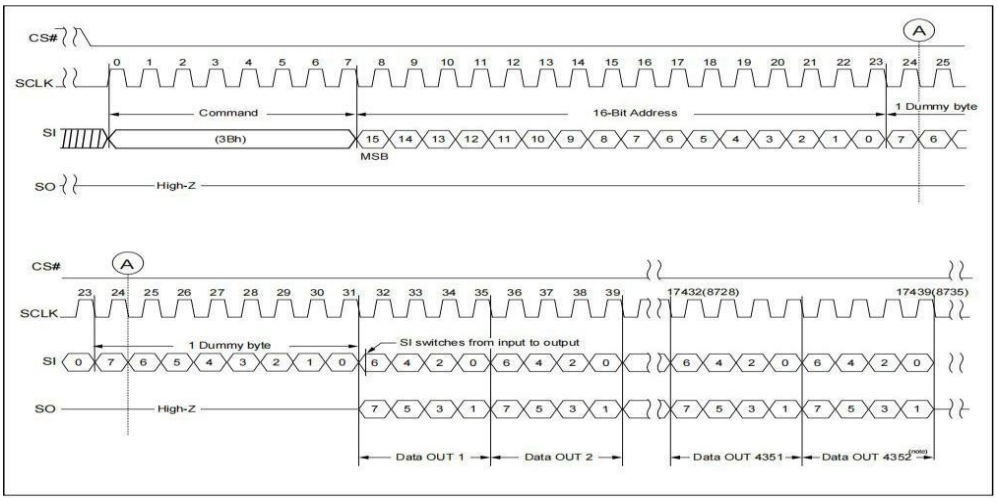
Figure 8-6.Read From Cache Timing Diagram



8.5 Read From Cache x2 (3BH)

The command sequence is shown below.

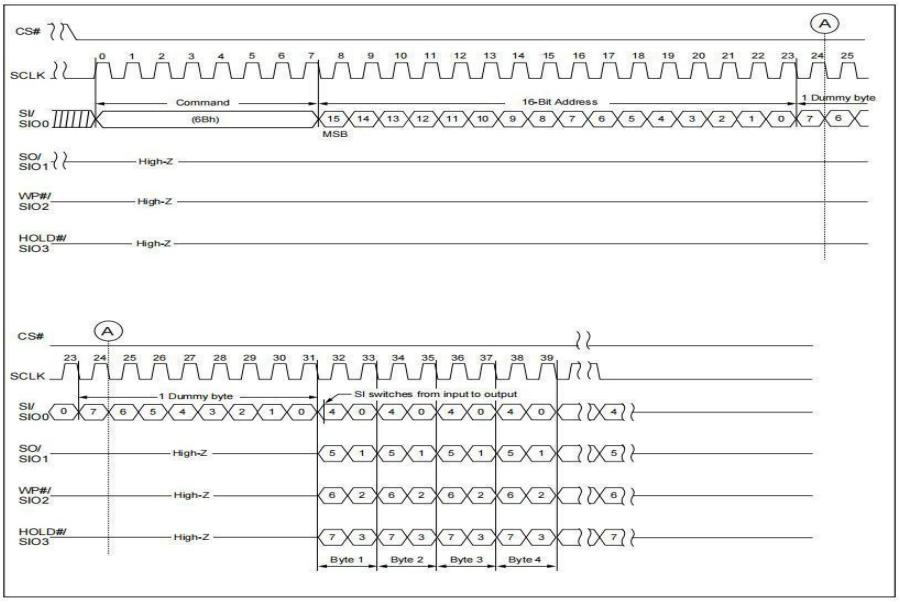
Figure 8-7.Read From Cache x2 Timing Diagram



8.6 Read From Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command. The command sequence is shown below.

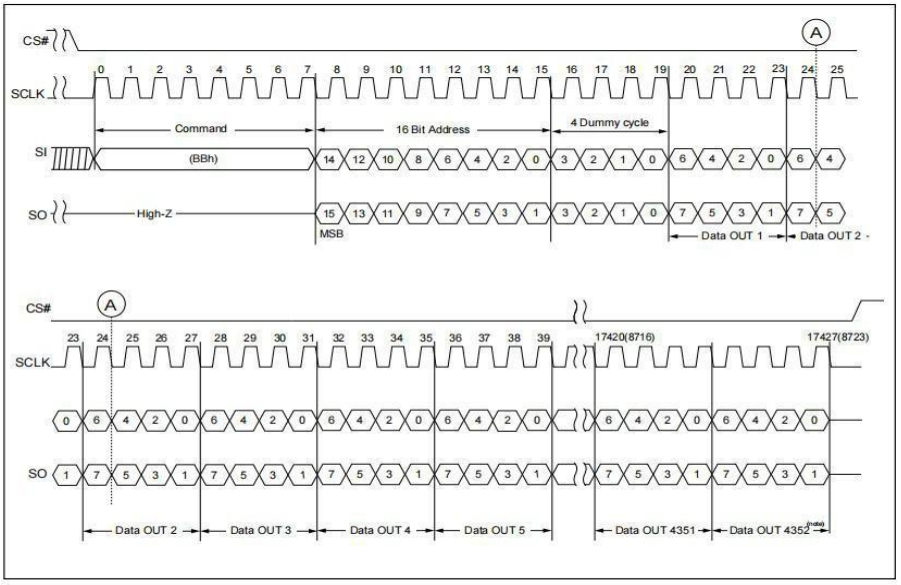
Figure 8-9.Read From Cache x4 Timing Diagram



8.7 Read From Cache Dual IO (BBH)

The Read from Cache Dual I/O command (BBH) is similar to the Read form Cache x2 command (3BH) but with the capability to input the 4 Dummy bits, followed by a 12-bit column address for the starting byte address and dummy bytes by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first address byte can be at any location. The address increments automatically to the next higher address after each byte of data shifted out. The command sequence is shown below.

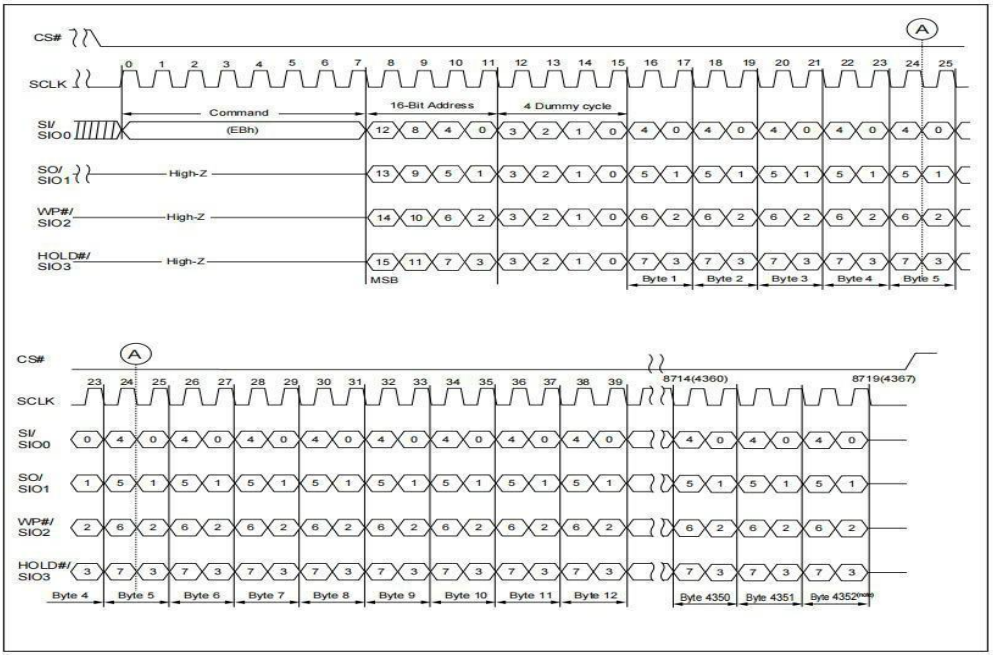
Figure 8-10.Read From Cache Dual IO Timing Diagram



8.8 Read From Cache Quad IO (EBH)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command but with the capability to input the 4 dummy bits, followed a 12-bit column address for the starting byte address and dummy bytes by SIO0, SIO1, SIO3, SIO4, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache quad IO command. The command sequence is shown below.

Figure 8-11.Read From Cache Quad IO Timing Diagram

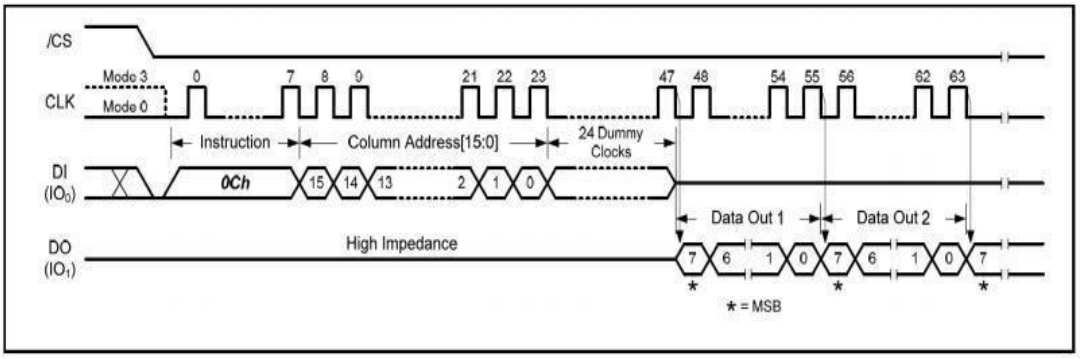


8.9 Read From Cache With 4Byte Address(0CH)

The Read From Cache instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read From Cache instruction is initiated by driving the CS# pin low and then shifting the instruction code –0ChII followed by the 16-bit Column Address and 24-bit dummy clocks into the DI pin.

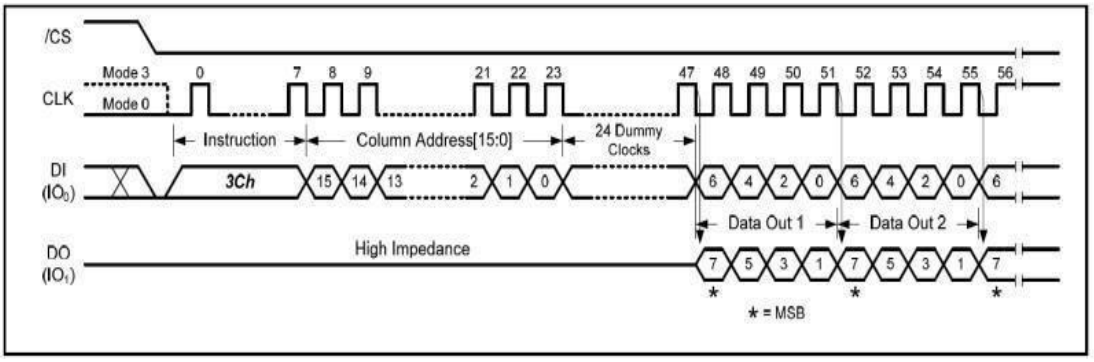
After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The instruction is completed by driving CS# high. The data output sequence will start from the Data Buffer location specified by the 16-bit Column •
Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state

Figure 8-12. Read From Cache With 4Byte Address Timing Diagram



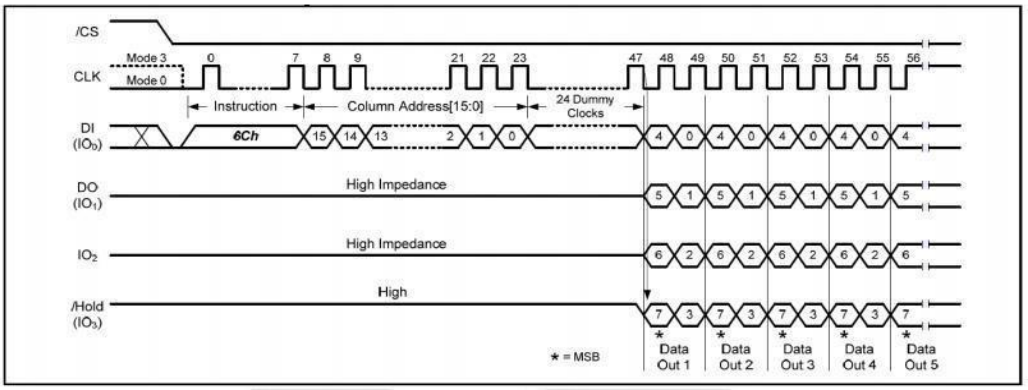
8.10 Read From Cache x2 With 4Byte Address (3CH)

Figure 8-13. Read From Cache x2 With 4Byte Address Timing Diagram



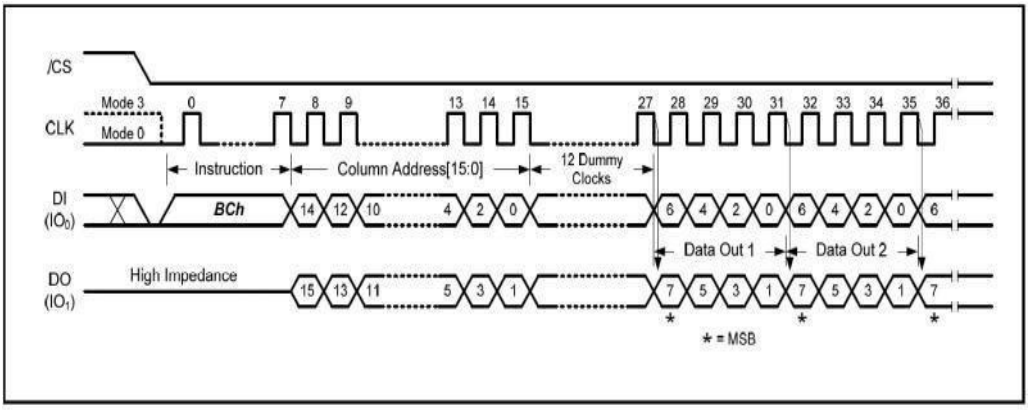
8.11 Read From Cache x4 With 4Byte Address (6CH)

Figure 8-14. Read From Cache x4 With 4Byte Address Timing Diagram



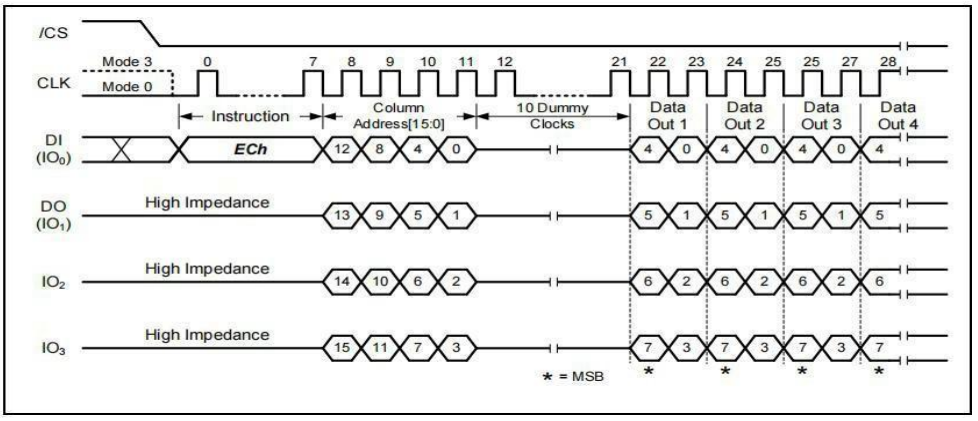
8.12 Read From Cache Dual IO With 4Byte Address (BCH)

Figure 8-15. Read From Cache Dual IO With 4Byte Address Timing Diagram



8.13 Read From Cache QUAD IO With 4Byte Address (ECH)

Figure 8-16. Read From Cache QUAD IO With 4Byte Address Timing Diagram



8.14 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device.

• With address 00H, the READ ID command outputs the Manufacturer ID and the device ID.

Figure 8-17.Read ID Timing Diagram

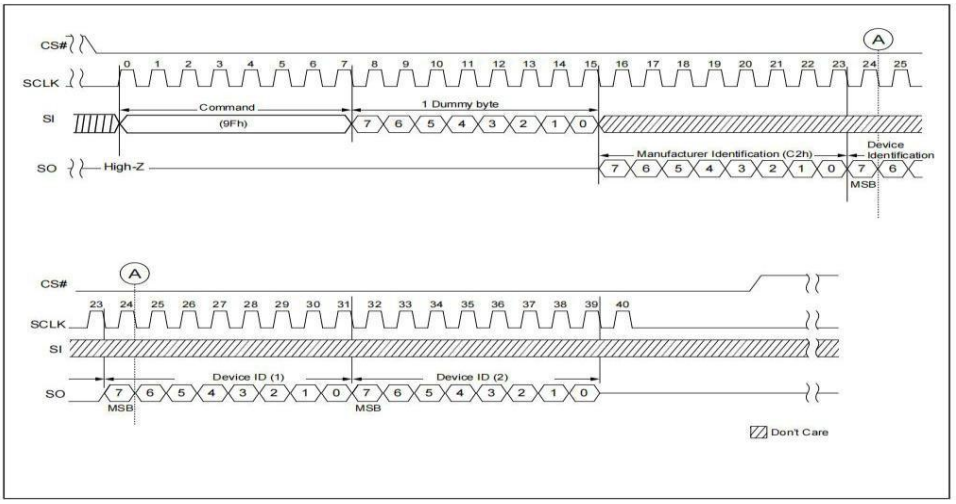


Table 8-2.READ ID Table

Part No	MID	DID1	DID2
MKSV1GIL-AE	F2h	0Ah	00
MKSV2GIL-AE	F2h	0Bh	00

8.15 Read UID

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall beunique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement are stored by the target. For example, reading byte 32-63 returns to the host another copy of the UID and its complement.

Table 8-3.UID Table

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 00h, read data from array to cache.
4. Use 0FH (GET FEATURES command) read the status.
5. User can use Read from cache command (03H/0BH), read 16 bytes UID from cache.

8.16 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. A minimum of three copies of the parameter page are stored in the device. The Read from Cache command can be used to change the location of data output.

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 01h. Load parameter page from array to cache.
4. Use 0Fh (GET FEATURES command) read the status
5. User can use Read from cache command (03h/0Bh), read parameter page from cache.

Table 8-4. Parameter page table as follow

<table>
<tr><th>Byte</th><th>O/M</th><th>Description</th><th>3.3V</th></tr>
<tr><td>0-3</td><td>M</td><td>Parameter pagesignature
Byte 0: 4FH, —Oǁ
Byte 1: 4EH, –Nǁ
Byte 2: 46H, –Fǁ
Byte 3: 49H, –Iǁ</td><td>4FH
4EH
46H
49H</td></tr>
<tr><td>4-5</td><td>M</td><td>Revision number
0-15 Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>6-7</td><td>M</td><td>Features supported
0-15 Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>8-9</td><td>M</td><td>Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>10-31</td><td></td><td>Reserved (0)</td><td>00H
…
00H</td></tr>
<tr><td></td><td></td><td>Manufacturer Information block</td><td></td></tr>
<tr><td>32-43</td><td>M</td><td>Device manufacturer (12 ASCII characters)</td><td>4cH
59H
00H
00H
00H
00H
00H
00H
00H
00H
00H
00H</td></tr>
<tr><td>44-63</td><td>M</td><td>Device model (20 ASCII characters)
<table>
<tr><th>Device Model</th><th>ORGANIZATION</th><th>VCC RANGE</th></tr>
<tr><td>MKSVxGIL-AE</td><td>X4</td><td>2.7v ~ 3.6v</td></tr>
</table></td><td>53H
50H
49H
4EH
41H
4EH
44H
00H
00H
00H
00H
00H
00H
00H
00H</td></tr>
</table>

			00H 00H 00H 00H 00H
64	M	JEDEC manufacturer ID-XXⅡ(MID)	FFH
65-66	O	Date code	00H 00H
67-79		Reserved	00H 00H 00H
		Memory organization block	
80-83	M	Number of data bytes per page	00H 10H 00H 00H
84-85	M	Number of spare bytes per page	00H 01H
86-89	M	Number of data bytes per partial page	00H 02H 00H 00H
90-91	M	Number of spare bytes per partial page	20H 00H
	M	Number of pages per block	40H 00H 00H 00H
96-99	M	Number of blocks per logical unit	00H 08H 00H 00H
100	M	Number of logical units	01H
101	M	Reserved	00H
102	M	Number of bits per cell	01H
103-104	M	Bad blocks maximum per logical unit	01H 00H
105-106	M	Block endurance	01H 05H
107	M	Guaranteed valid blocks at beginning of target	08H

108-109	M	Block endurance for guaranteed valid blocks	00H 00H
110	M	Number of programs per page	04H
111	M	Partial programmingattributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00H
112	M	Number of bits ECC correctability	00H
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00H
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00H
115-127		Reserved	00H … 00H
		Electrical parameters block	
128	M	I/O capacitance	06H
129-130	M	IO clock support 3-1 5 Reserved (0) 2 1 = supports 80MHz 1 1 = supports 104MHz 0 1 = supports 120MHz	02H 00H
131-132	O	Reserved (0)	00H 00H
133-134	M	tPROG Maximum page program time (us)	20H 03H
135-136	M	tBERS Maximum block erase time (us)	10H 27H
137-138	M	tR Maximum page read time (us)	C2H 01H
139-140	M	Reserved	00H 00H
141-163		Reserved	00H
		Vendor block	
164-165	M	Vendor specific Revision number	00H
166-253		Vendor specific	00H
254-255	M	Integrity CRC	Set on test
		Redundant parameter pages	

256-511	M	Value of bytes 0-255	
512-767	M	Value of bytes 0-255	
768+	O	Additional redundant parameter pages	

Notes:

1. —Ol Stands for Optional, –Ml for Mandatory
2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details. The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X^{16} + X^{15} + X^{2} + 1$， This polynomial in hex may be represented as 8005h.

3. The CRC valueshall be initialized with a value of 4F4Eh before the calculation begins. There is noXOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

9 PROGRAM OPERATIONS

9.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to whole page bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Firstly, a PROGRAM LOAD (02H/32H) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by column address, then the data bytes to be programmed. The Program address should be in sequential order in a block. The data bytes are loaded into a cache register that is whole page long. If more than one page data are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 9-1 shows the PROGRAM LOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

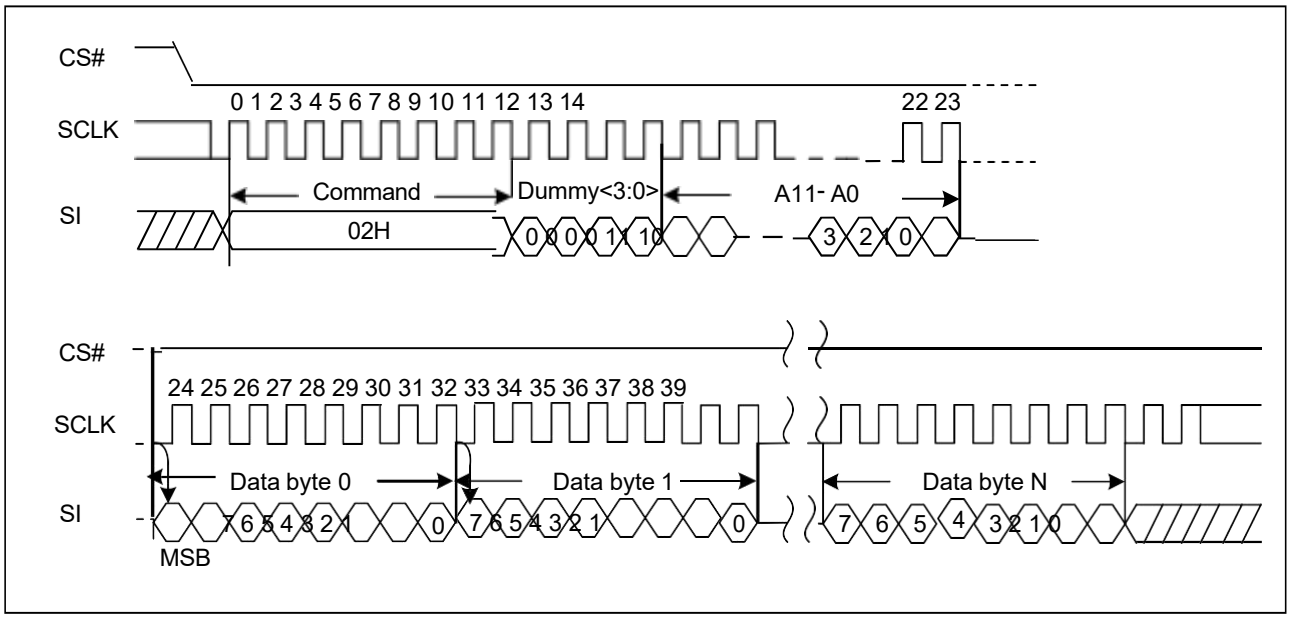
Note:

1. The contents of Cache Register don‘t reset when Program Random Load (84h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h) command, the 0xFF is output to the address that data was not loaded by Program Load (02h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h) command, the contents of Cache Register are output to the NAND array.
4. The Program address should be in sequential order in a block.
5. Program Load x4 is only available with the QE enable.

9.2 Program Load (PL) (02H)

The command sequence is shown below.

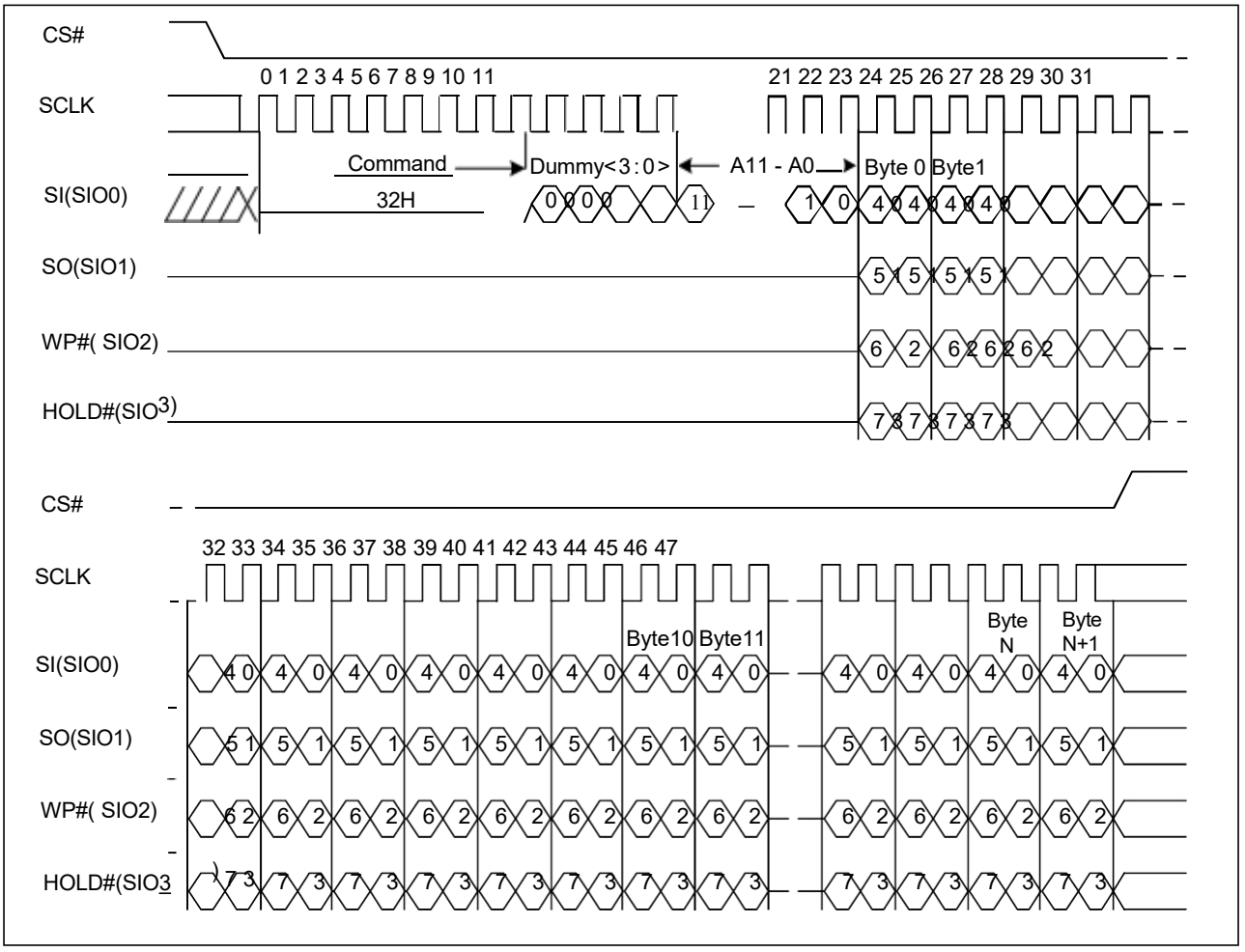
Figure 9-1. Program Load Timing Diagram



9.3 Program Load x4 (PL x4) (32H)

The Program Load x4 command (32H) is similar to the Program Load command (02H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command. The command sequence is shown below.

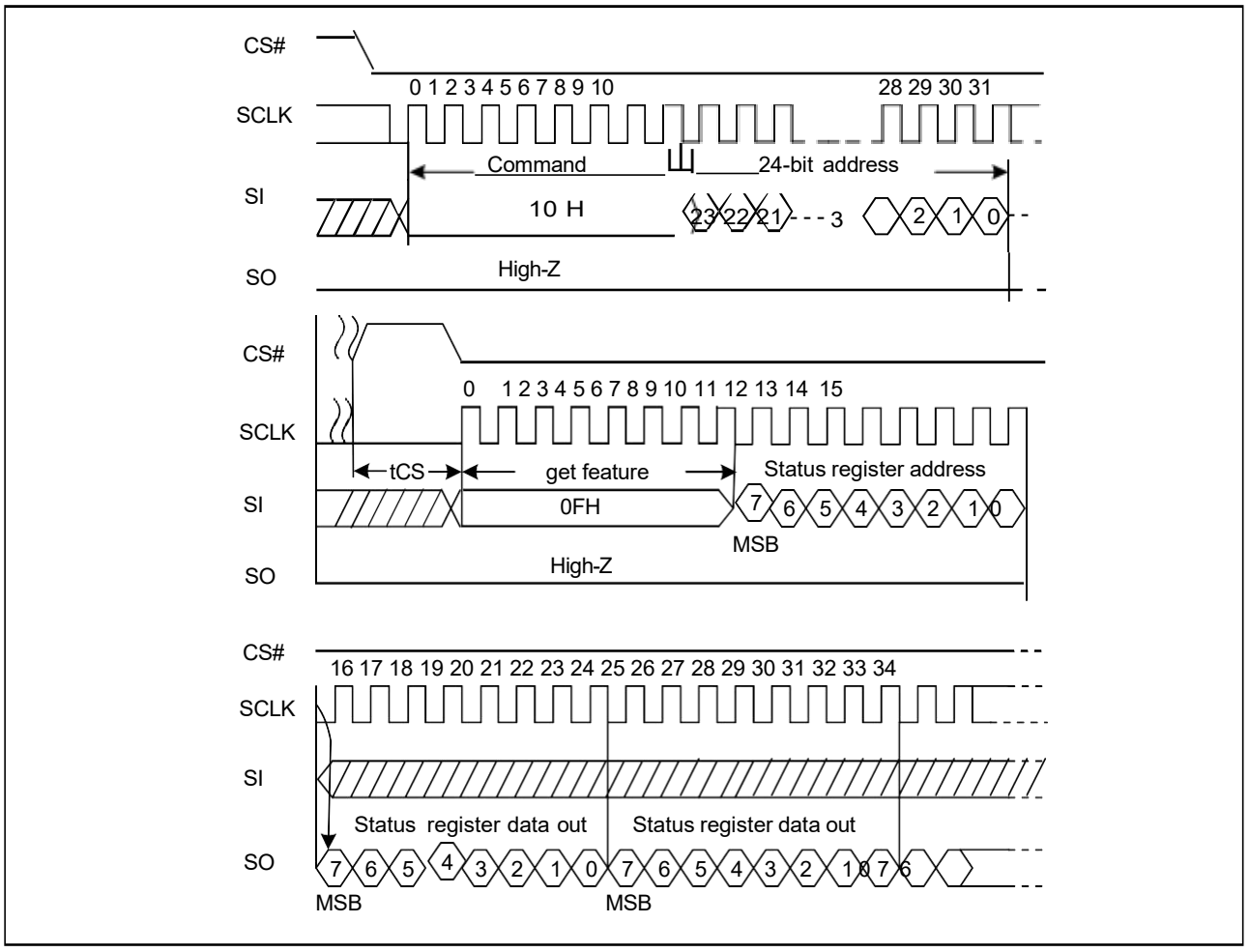
Figure 9-2.Program Load x4 Timing Diagram



9.4 Program Execute (PE) (10H)

After the data is loaded, a PROGRAM EXECUTE (10H) command must be issued to initiate the transfer of data from the cache registers to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation shown in Figure 9-3. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure 9-3.Program Execute Timing Diagram



9.5 Program Execute Background (10H + address + 15H)(15H + address)

A ‐Cache Program‖ function has been implemented in SPI series to improve the overall program throughput. It is possible to program the data from Data Register to array the simultaneously while a Load Data command is being performed to write data to the Cache Register.

When multiple pages of data is to be program sequentially or random, the host should issue a ‐Program Load (02h)‖ command followed by a Column Address and data written. When the command is accepted, the host should use Program Execute

Background command to initial the internal program operation, then the CBSY becomes 1.

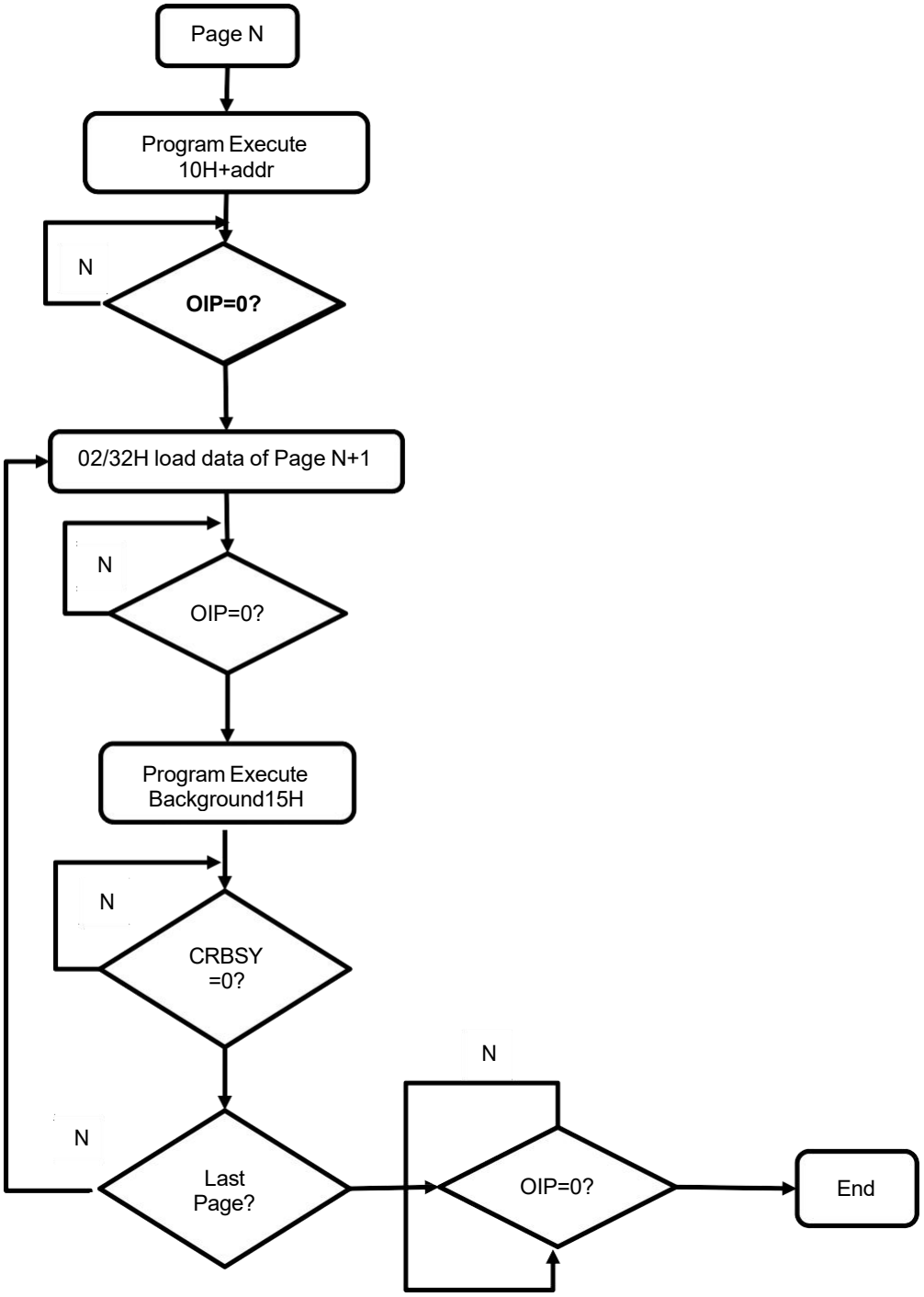
Once the CBSY becomes 0, user can issue again the ‐Program Load (02h)‖ command followed by a Page Address and data written. Then user can send Program Execute Background command to continue the cache program.

When the last page to be program, to guarantee data have programed, the OIP bit must become 0.

The Program Execute Background is allowed to cross blocks before reaching the last block.

1• 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
2• 06H (WRITE ENABLE)
3• 15H (PROGRAM EXECUTE)
4• 0FH (GET FEATURE command to read the status) wait CBSY=0
5• 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
6• 0FH (GET FEATURE command to read the status) wait OIP=0
7• Repeat step 2~6 until last page
8• 0FH (GET FEATURE command to read the status) wait OIP=0 to guarantee data of last page have programed

Figure 9-4.Program Execute Background Sequential Timing



Diagram

Figure 9-5.Program Execute Background Random Timing Diagram

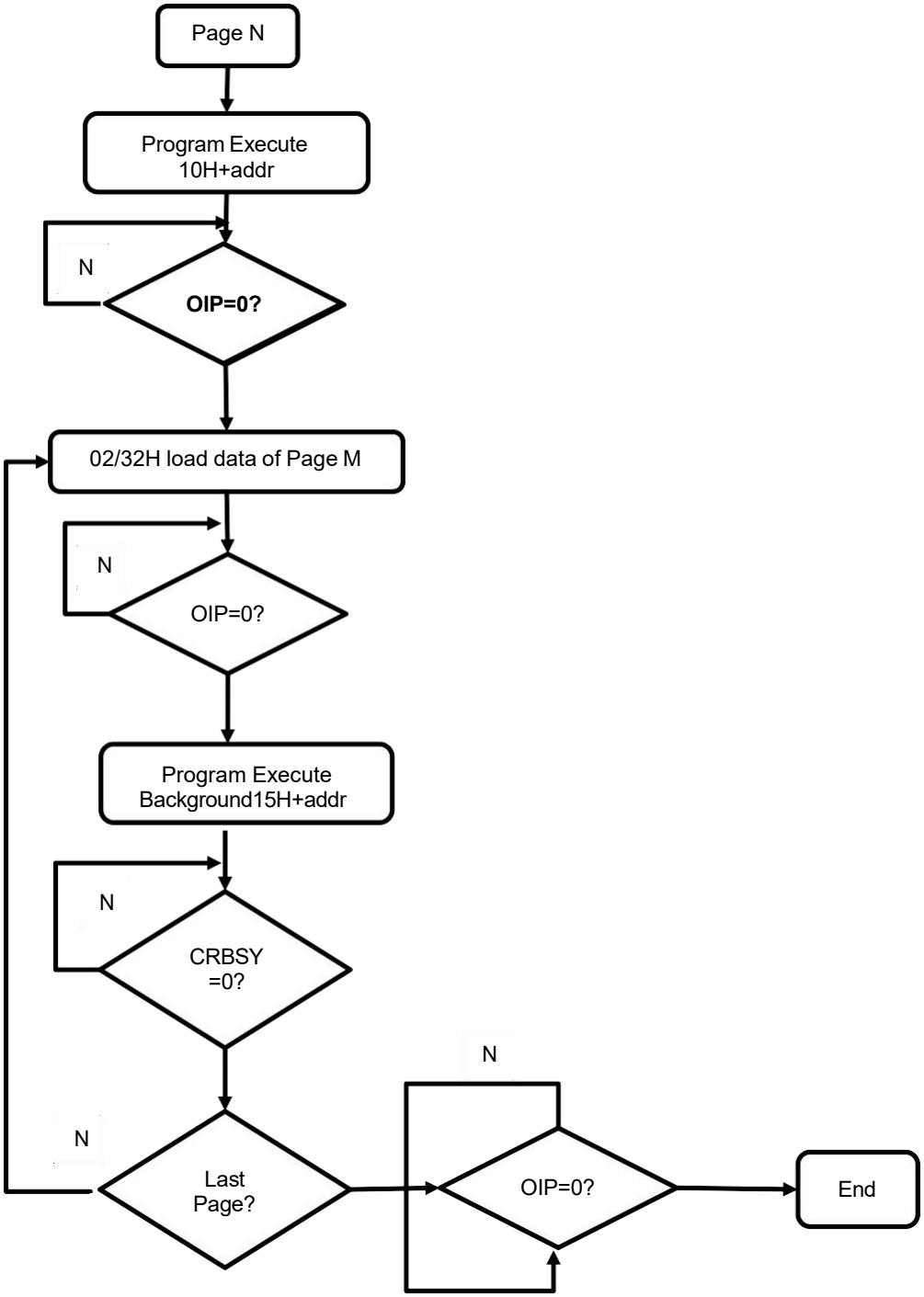
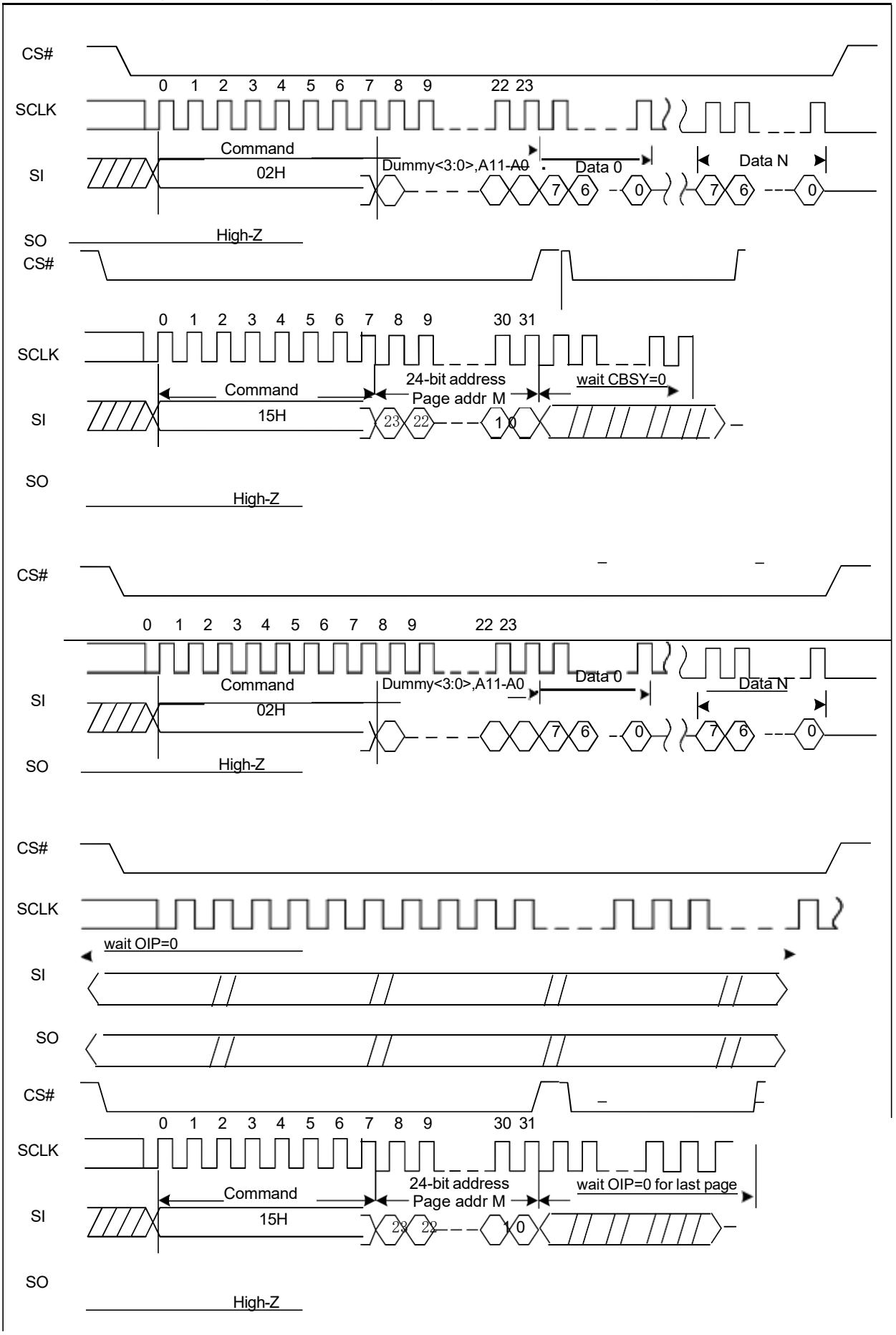


Figure 9-6.Program Execute Background Random Cycle Diagram



9.6 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is asfollows:

- 13H (PAGE READ to cache)
- Optional 84H/C4H/34H/72H (PROGRAM LOAD RANDOM DATA)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read thestatus)

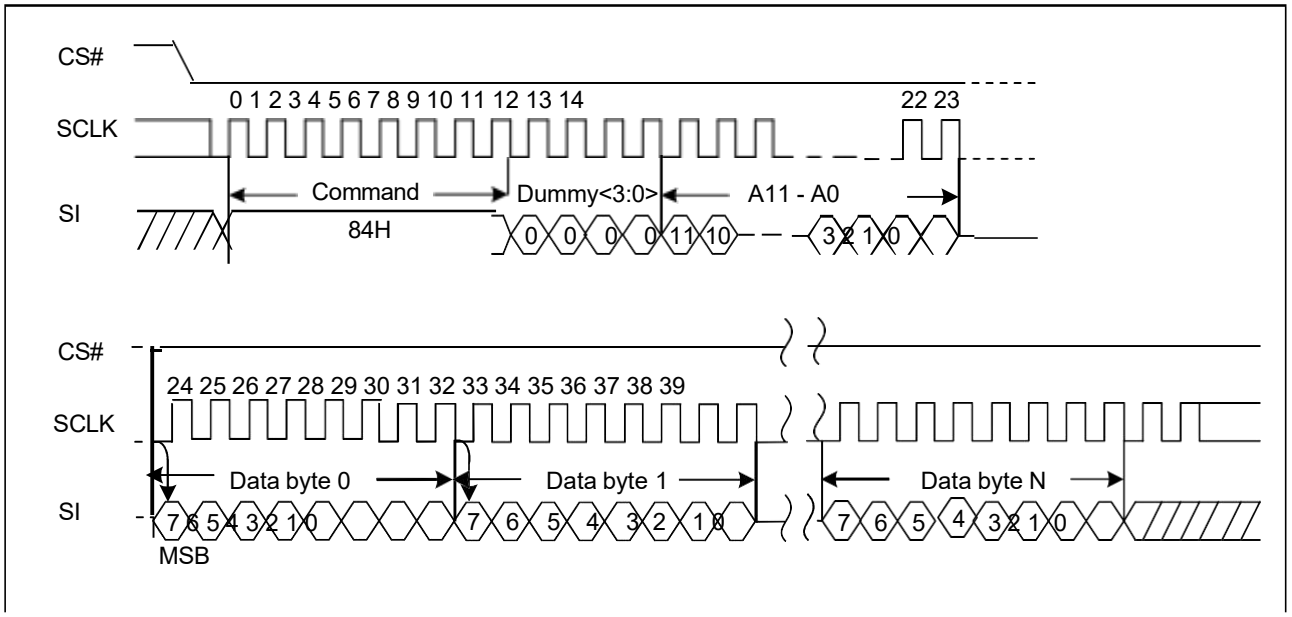
Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command can be issued, if user wants to update bytes of data in the page. New data is loaded in the 12/13-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then PROGRAMEXECUTE (10H) command can be issued to start the programming operation.

The most significant difference is program load operation reset data that not be addressed to FFh but program load random data operation not.

9.7 Program Load Random Data (84H)

The Program Load Random Data command programs or replaces data in a page with existing data. This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84H) command must be issued with a new column address.

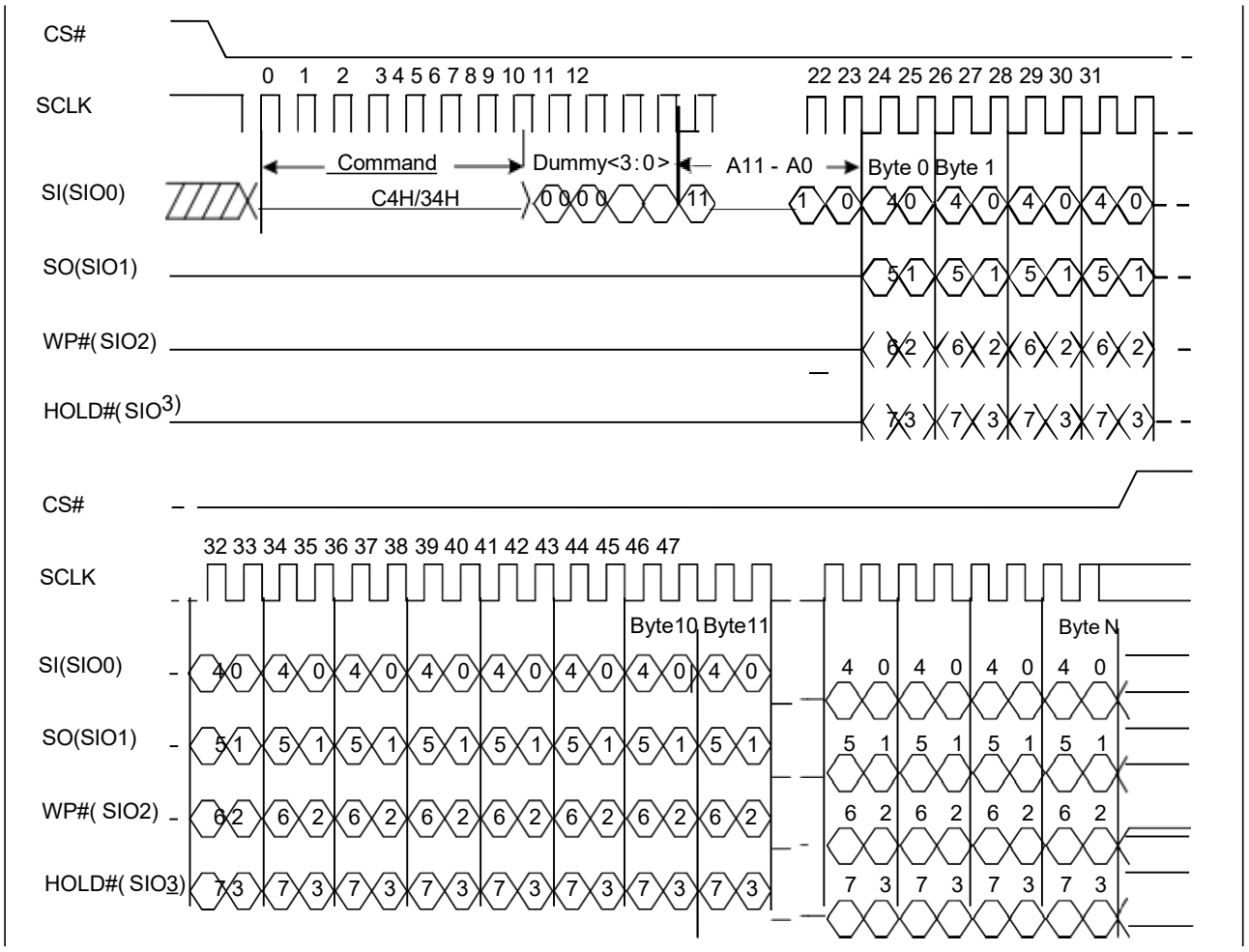
Figure 9-7.Program Load Random Data Timing Diagram



9.8 Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 command (C4H/34H) is similar to the Program Load Random Data command (84H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command.

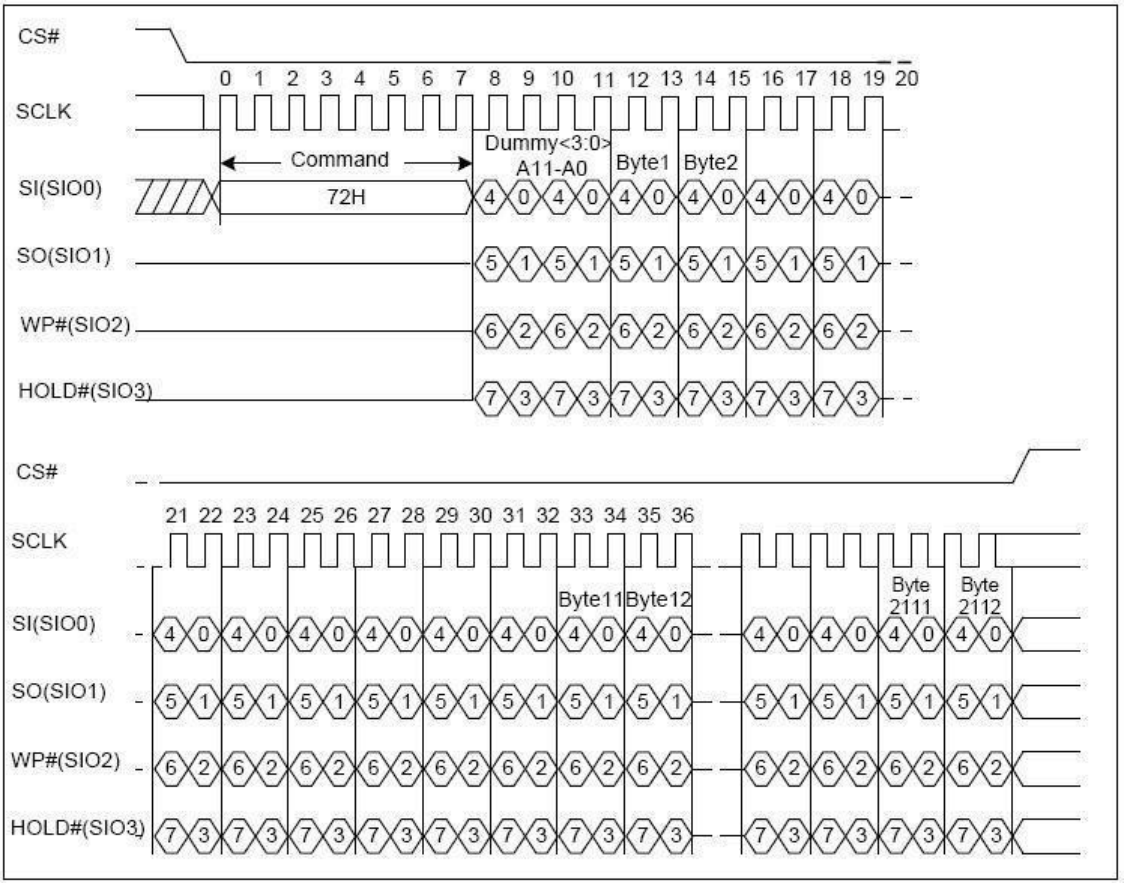
Figure 9-8.Program Load Random Data x4 Timing Diagram



9.9 Program Load Random Data Quad IO (72H)

The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable.

Figure 9-9. Program Load Random Data Quad IO Timing Diagram



10 ERASE OPERATIONS

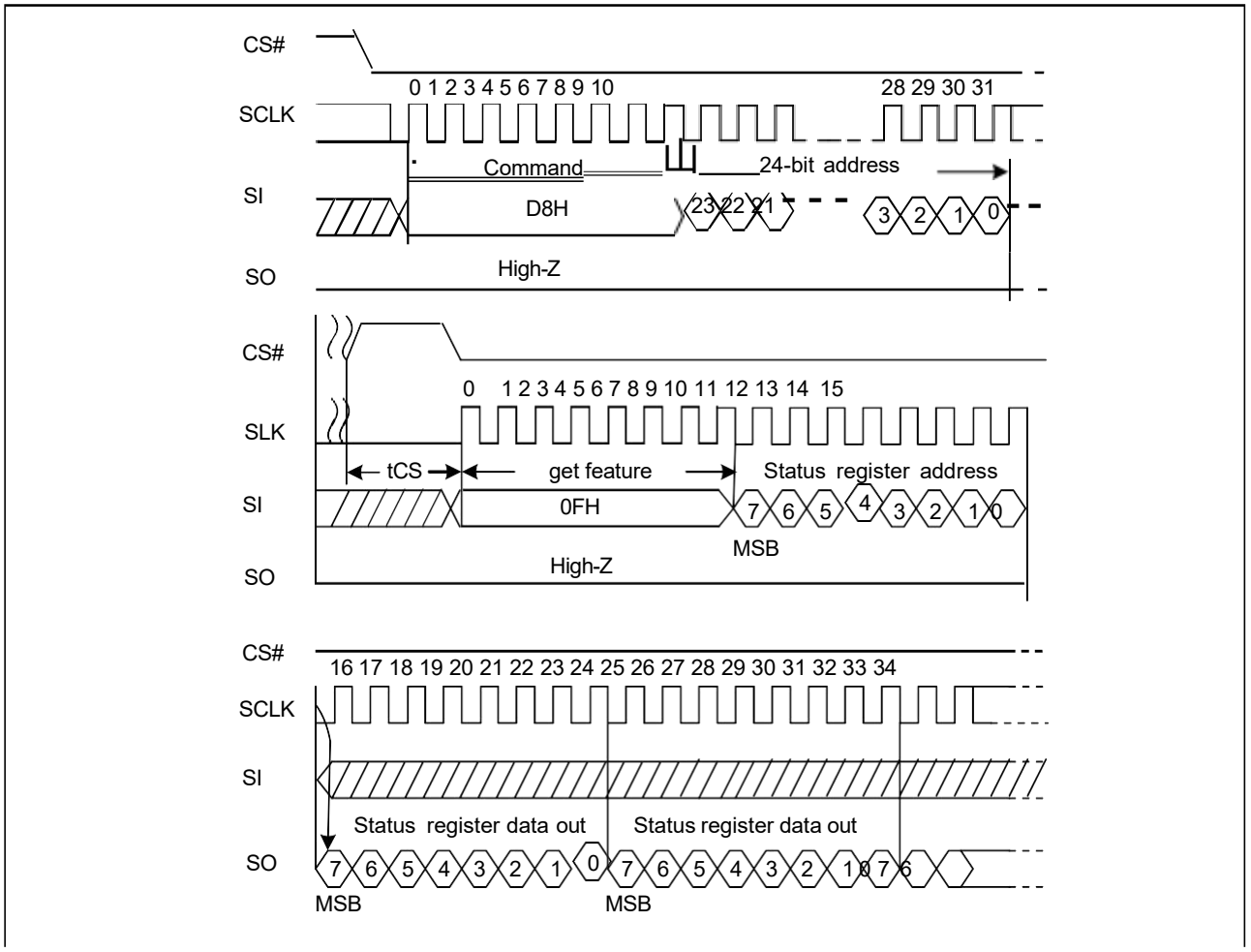
10.1 Block Erase (D8H)

The BLOCK ERASE (D8H) command is used to erase at the block level. The BLOCK ERASE command (D8H) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06H (WRITE ENBALE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, the WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. The WRITE ENABLE command must be followed by the BLOCK ERASE (D8H) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tBERS time during the BLOCK ERASE operation. The GET FEATURES (0FH) command can be used to monitor the status of the operation.

Figure 10-1.Block Erase Timing Diagram



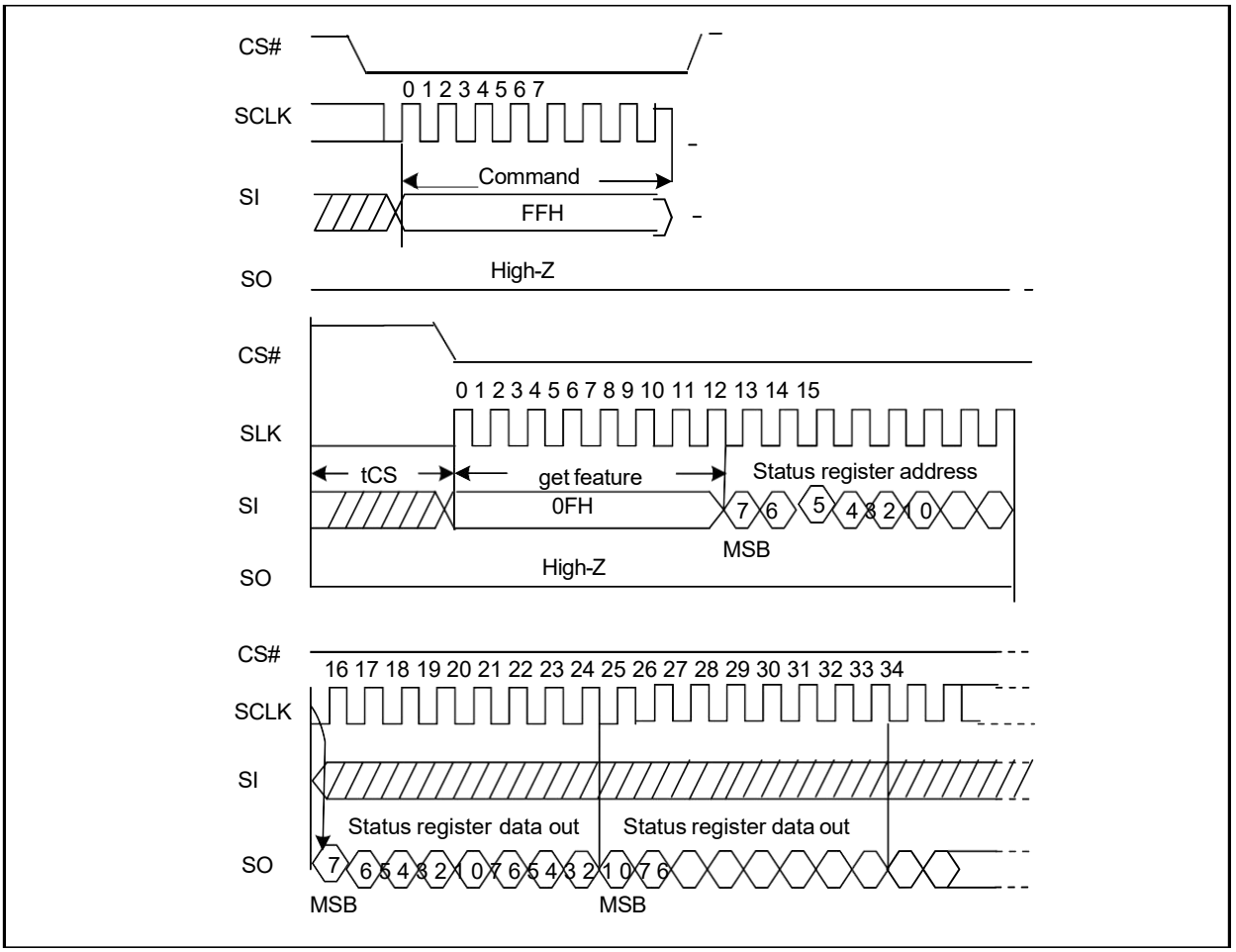
11 RESET OPERATIONS

11.1 Soft Reset (FFH)

The RESET (FFH) command stops all operations and the status. For example, in case of a program or erase or read operation, the reset command can make the device enter the idle state.

During a cache program or cache read, a reset can also stops the previous operation and the pending operation.

Figure 11-1.Reset Timing Diagram

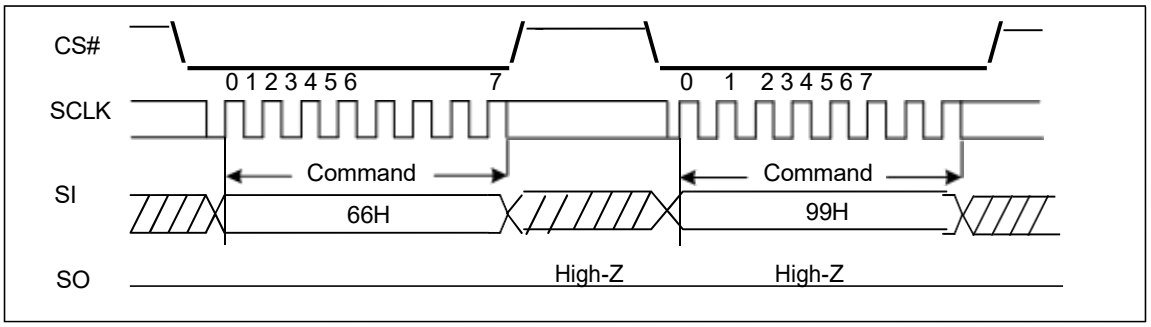


11.2 Enable Power on Reset (66H) and Power on Reset (99H)

If the Power on Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current feature settings.

The —Enable Reset (66H)‖ and the —Reset (99H)‖ commands can be issued in SPI mode. The —Reset (99H)‖ command sequence as follow: CS# goes low -> Sending Enable Reset command ->CS# goes high ->CS# goes low.->Sending Reset command ->CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tVSL to reset. During this period, no command will be accepted. The contents of the memory location being programmed or the block being erased are no longer valid.

Figure 11-2.Reset Timing Diagram



12 FEATURE OPERATIONS

12.1 Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Feature such as OTP can be enabled or disabled by setting specific feature bits (shown in the below table).The status registers (C0H/F0H) is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06H) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFH) command is issued.

Table 12-1.Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	BUF	Reserved	Reserved	QE
Status	C0H	CBSY	LUTF	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	HSOS	DS_IO[1]	DS_IO[0]	Reserved	Reserved	Reserved	ECCSE1	ECCSE0
Feature	10H	BFD7	BFD6	BFD5	BFD4	BFD3	BFD2	BFD1	BFD0
Feature	20H	BFS7	BFS6	BFS5	BFS4	BFS3	BFS2	BFS1	BFS0

Note: 1. If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

2. If QE is enabled, the quad IO operations can be executed.
3. All the reserved bits must be held low when the feature is set.
4. These registers A0H/B0H/D0H are write/read type, and Registers C0H/F0H are read only.
5. The OTP_PRT is non-volatile, others bits are volatile.
6. The Register Bit default value after power-up refers to Table 12-2. Register Bit Descriptions.

Table 12-2. Register Bit Descriptions

Bit	Bit Name	After Power up or Power on Reset(66H-99H)	After Reset command (FFH)	Description
BRWD	Block register write disable	0	No Change	Which is used combined with WP#, If BRWD is high enabled and WP# is LOW, then the Protection register cannot be changed
BP2 BP1 BP0 INV CMP	Block Protection bits	1 1 1 0 0	No Change	Used combination, refer to chapter Block Protection
OTP_PRT OTP_EN	OTP Region bits	0 0 Before OTP Set	No Change	Used combination, refer to chapter OTP Region
ECC_EN	ECC Enable Latch	1	No Change	The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the ‐activeǁ state when ECC enable.
BUF	Continuous Read	1	No Change	0: Continuous read 1: Normal read
QE	The Quad Enable bit	0	No Change	This bit indicates that whether the quad IO operations can be executed. If QE is set to 1, the quad IO operations can be executed.
ECCS0 ECCS1 ECCSE0 ECCSE1	ECC Status	Page 0 Status	0 0 0 0	ECCS provides ECC status as the following table. ECCS and ECCSE are set to 00b either following a RESET, or at the beginning of the READ. They are then updated after the device completes a valid READ operation. ECCS and ECCSE are invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN to 0). After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.
P_FAIL	Program Fail	0	0	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).

E_FAIL	Erase Fail	0	0	This bit indicates that an erase failure has occurred (E_FAIL = 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	0	0	This bit indicates the current status ofthe write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	0	0	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
HSOD	Data rising edge output	0	No Change	This bit control data output edge to achieve higher access speed than nominal speed by SO. This bit is default _0‘ after power on and data output with rising edge is valid only in SPI MODE0. When HSOD is _1‘, user should latch data by rising edge without sample-shifting while accessing memory by SO. _0‘ is falling edge output. _1‘ is rising edge output.
DS_IO[0] DS_IO[1]	Driven Strength register	0 1	No Change	IO driver strength setting. Default is 00b.
BPS	Block Protection Status	1	No Change	Block protection status BPS is 1, selected block is protected BPS is 0, selected block is unprotected.
CBSY	Cache Busy status bit	0	0	CBSY is to indicate whether cache is busy, non-available for data read or data load. This bit is the status, which indicates if the cache is busy or ready, 1 is busy, 0 is ready.
LUTF	BBM Full	BBM Status	No Change	1 is Full
BFD	ECC Bit Flip Count Detection	All 1		The ECC Bit Flip Count Detection function detects the bit flip count in a page. The users set the threshold bit count using BFD feature. The detected results will be indicated in the BFS bits. BFD should not over ECC correction ability.
BFS	Sector ECC over ECC bit flip count			When bit flips exceed the threshold in a sector, the BFS bits are set after the Page Data Read (13h) command with ECC_EN =1.

Table 12-3. BFD Bit Descriptions

BFD BITS	Detect ECC flip bit
00H	Ecc flip bit disable
01H	Detect 1 bit flip in a sector
02H	Detect 2 bit flip in a sector
03H	Detect 3 bit flip in a sector
04H	Detect 4 bit flip in a sector
05H	Detect 5 bit flip in a sector
……	……

Table 12-4. BFS Bit Descriptions

BFSn BIT	Description
0	Sector n detect error bit less than BFD & correctable
1	Sector n detect error bit more than or equal to BFD bit error

Figure 12-1.Get Features TimingDiagram

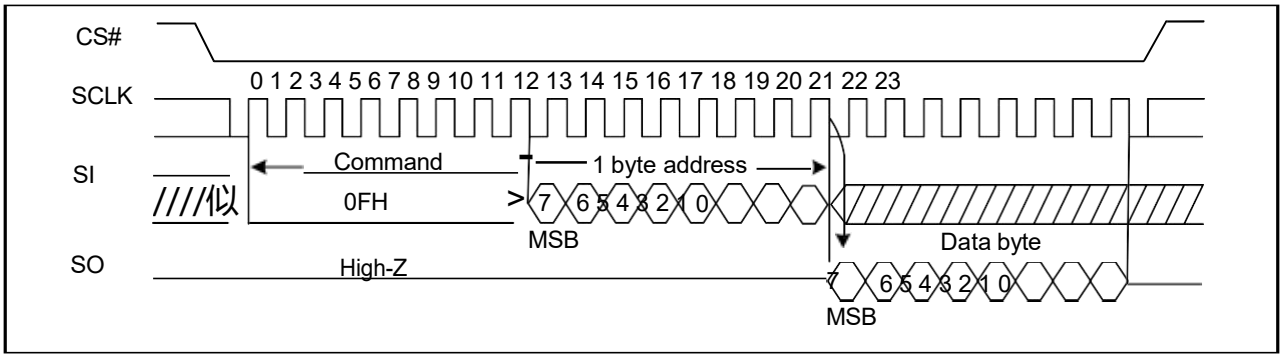


Figure 12-2.Set Features TimingDiagram

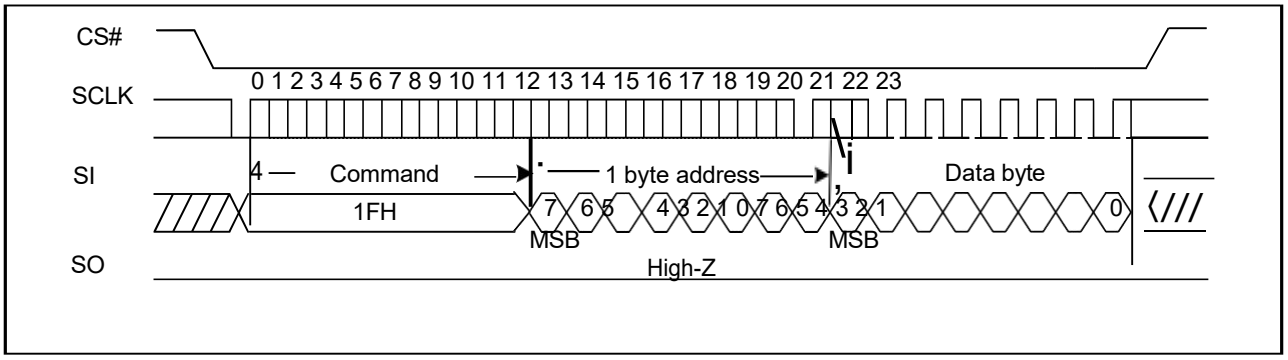
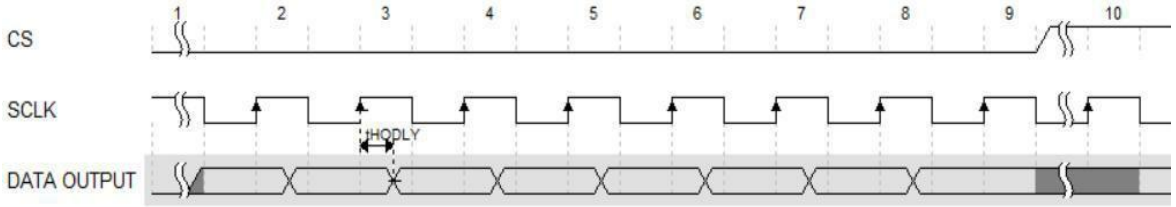


Figure 12-3.HSOD=1 Data Rising Edge Output Timing Diagram



12.2 Status Register and Driver Register

The NAND Flash device has status registers (C0H/F0H) that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH) command, followed by the feature address C0H or F0H (see FEATURE OPERATION). The Output Driver Register can be set and read by issuing the SET FEATURE (0FH) and GET FEATURE command followed by the feature address D0H (see FEATURE OPERATION).

Table 12-5.ECC Error Bits Descriptions

ECC Ability	ECCS1	ECCS0	ECCSE1	ECCSE0	Description
16	0	0	x	x	No bit errors were detected during the previous read algorithm
	0	1	0	0	1~2 Bit errors were detected and corrected
	0	1	0	1	3~4 Bit errors were detected and corrected.
	0	1	1	0	5~6 Bit errors were detected and corrected.
	0	1	1	1	7~8 Bit errors were detected and corrected.
	1	0	0	0	9~10 Bit errors were detected and corrected.
	1	0	0	1	11~12 Bit errors were detected and corrected.
	1	0	1	0	13~14 Bit errors were detected and corrected.
	1	0	1	1	15~16 Bit errors were detected and corrected.
	1	1	x	x	Bit errors greater than ECC capability and not corrected

Table 12-6.Driver Register Bits Descriptions

DS_IO[1]	DS_IO[0]	Driver Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%

12.3 OTP Region

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 8 full pages are available on the device. Customers can use the OTP area as they prefer, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0. To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, only pages 02h–0AH can be programmed in sequential order by PROGRAM LOAD (02H) and PROGRAM EXECUTE (10H) commands (when not yet protected), and read out by PAGE READ (13H) command and output data by READ from CACHE(03H/0BH/3BH/6BH).When ECC is enabled, data written in the OTP area is ECC protected.

Note: OTP page 0,1 is UID page and parameter page. They are not allowed to be program.

Table 12-7.OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region, read and program data
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

Access to OTP data

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0FH command.

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command.

12.4 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the –locked‖ state, i.e., feature bits BP0, BP1and BP2 are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0. When an ERASE command is issued to a locked block, the erase failure, status bit E_FAIL set to 1. When a PROGRAM command is issued to a locked block, program failure, status bit P_FAIL set to 1.

To enable the Write Protection (WP#), the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

Table 12-7.Block Lock Register Block Protect Bits

CMP	INV	BP2	BP1	BP0	Protect Rows
x	x	0	0	0	None—all unlocked
0	0	0	0	1	Upper 1/64 locked
0	0	0	1	0	Upper 1/32 locked
0	0	0	1	1	Upper 1/16 locked
0	0	1	0	0	Upper 1/8 locked
0	0	1	0	1	Upper 1/4 locked
0	0	1	1	0	Upper 1/2 locked
x	x	1	1	1	All locked (default)
0	1	0	0	1	Lower 1/64 locked
0	1	0	1	0	Lower 1/32 locked
0	1	0	1	1	Lower 1/16 locked
0	1	1	0	0	Lower 1/8 locked
0	1	1	0	1	Lower 1/4 locked
0	1	1	1	0	Lower 1/2 locked
1	0	0	0	1	Lower 63/64 locked
1	0	0	1	0	Lower31/32 locked
1	0	0	1	1	Lower 15/16 locked
1	0	1	0	0	Lower7/8 locked
1	0	1	0	1	Lower3/4 locked
1	0	1	1	0	Block0
1	1	0	0	1	Upper 63/64 locked
1	1	0	1	0	Upper31/32 locked
1	1	0	1	1	Upper 15/16 locked
1	1	1	0	0	Upper7/8 locked
1	1	1	0	1	Upper3/4 locked
1	1	1	1	0	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue SET FEATURES register write (1FH)
- Issue the feature bit address (A0h) and the feature bits combination as the table.

12.5 Internal ECC

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the —activeǁ state when ECC enable.

To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1FH) to set the feature bit ECC_EN:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. Iferror bits are detected (error bits≤4 bits), the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page. The ECC protection format asfollow:

- User meta data I is not protected by internal ECC and User meta data II is protected by internal ECC.

Table 12-9. The Distribution of ECC Segment and Spare Area in a Page

Main0	Main1	Main2	Main3
(512B)	(512B)	(512B)	(512B)
user	user	user	user
Spare(0)	Spare(1)	Spare(2)	Spare(3)
16Byte	16Byte	16Byte	16Byte
user	user	user	user
Spare2(0)	Spare2(1)	Spare2(2)	Spare2(3)
16Byte	16Byte	16Byte	16Byte
ECC	ECC	ECC	ECC

Table 12-10. ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC Protected	Area	Description
000H	1FFH	Yes	Main 0	User data 0
200H	3FFH	Yes	Main 1	User data 1
400H	5FFH	Yes	Main 2	User data 2
600H	7FFH	Yes	Main 3	User data 3
800H	80FH	Yes	Spare 0	User meta 0 data & Bad Block Mark
810H	81FH	Yes	Spare 1	User meta 1 data
820H	82FH	Yes	Spare 2	User meta 2 data
830H	83FH	Yes	Spare 3	User meta 3 data
840H	84FH	Yes	Spare2-0	ECC parity data 0
850H	85FH	Yes	Spare2-1	ECC parity data 1
860H	86FH	Yes	Spare2-2	ECC parity data 2
870H	87FH	Yes	Spare2-3	ECC parity data 3

Note

1. 800H(2K page size) is reserved for initial bad block mark.
2. When Internal ECC is disabled, we recommend the user to provide external ECC protection
3. Mark is reserved for ECC parity datas

13 Block Management

13.1 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (NVB) of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFH data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

To simplify the system requirement and guard the data integration, SPI NAND provides assistant Management options as below.

Table 13-1.Bad Block Mark information

Description	Requirement
Minimum number of valid blocks (NVB)	1004/2008
First spare area location	Byte 2048
Bad-block mark	00h(use non FFH to check)

13.2 Bad Block Management (BBM)(A1h)

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of –Bad Blocks‖ found in the factory testing.In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A –Bad Block Marker‖ is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first byte of spare area.

FT spi-nand offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The –Bad Block Management‖ command is initiated by shifting the instruction code –A1h‖ into the DI pin and followed by the 16-bits -Logical Block Address‖ and 16-bits -Physical Block Address‖. The logical block address is the address for the —bad‖ block that will be replaced by the –good‖ block indicated by the physical block address.

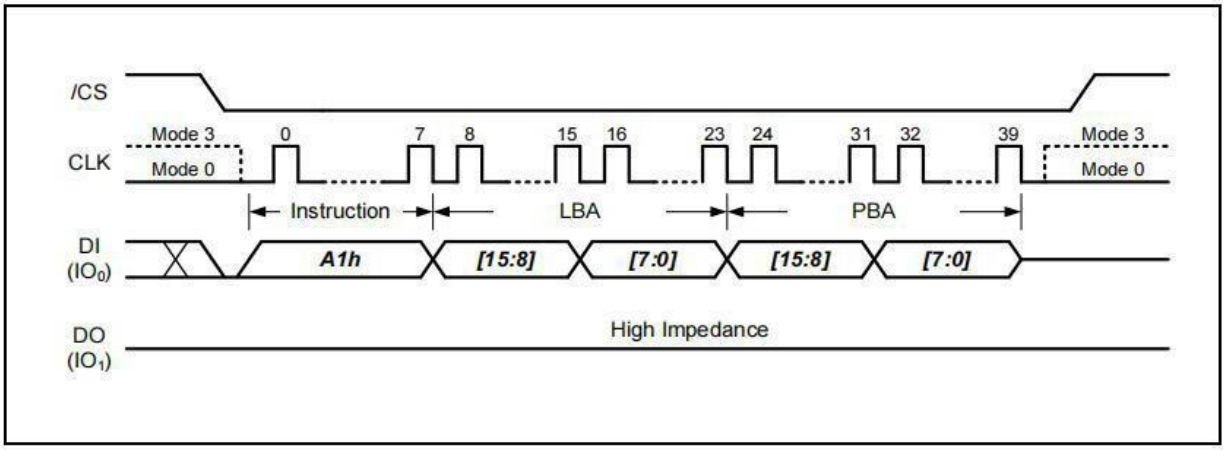
The Bad Block Management instruction is initiated by driving the /CS pin low and shifting the instruction code –A1h‖ followed by 16-bits LBA (Bad Block address) and the 16-bits PBA (Good Block address). After /CS is driven high to complete the instruction cycle, the OIP bit will become a 1 while the Bad Block Management cycle is in progress.The Read Status Register instruction should be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Bad Block Management cycle and becomes a 0 when the cycle is finished

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 10 links can be established in the non-volatile LUT. If all 10 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a –Read BBM Look Up Table‖ command can be issued to confirm if spare links are still available in the LUT.

If device support Continuous Read Operation, to guarantee a continuous read operation on the first 1,000 blocks, the manufacturer may have used some of the BBM LUT entrees. It is advisable for the user to scan all blocks and keep a table of all manufacturer bad blocks prior to first erase/program operation.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

Figure 13-1.BBM Timing Diagram



13.3 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 20 Logical-Physical memory block links (from LBA0/PBA0 to LBA19/PBA19). The ‐Read BBM Look Up Table‖ command can be used to check the existing address links stored inside the LUT.

The ‐Read BBM Look Up Table‖ command is initiated by shifting the instruction code ‐A5h‖ into the DI pin and followed by 8-bits dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bits ‐Logical Block Address‖ and the 16-bits ‐Physical Block Address‖. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all ‐00h‖ data.

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

Figure 13-2.Read BBM Timing Diagram

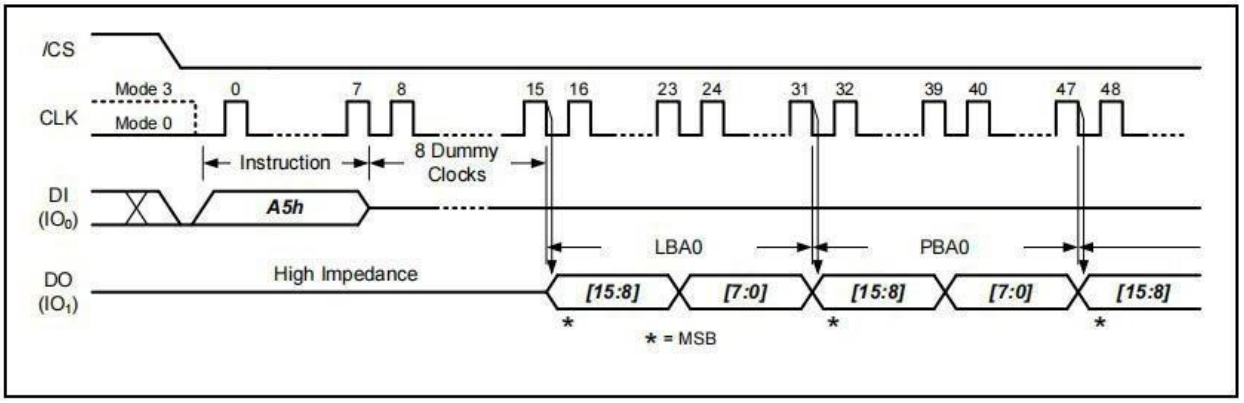


Table 13-2.Read BBM Markinformation

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled and it is a valid link.
1	1	This link was enabled, but it is not valid any more.
0	1	Not applicable.

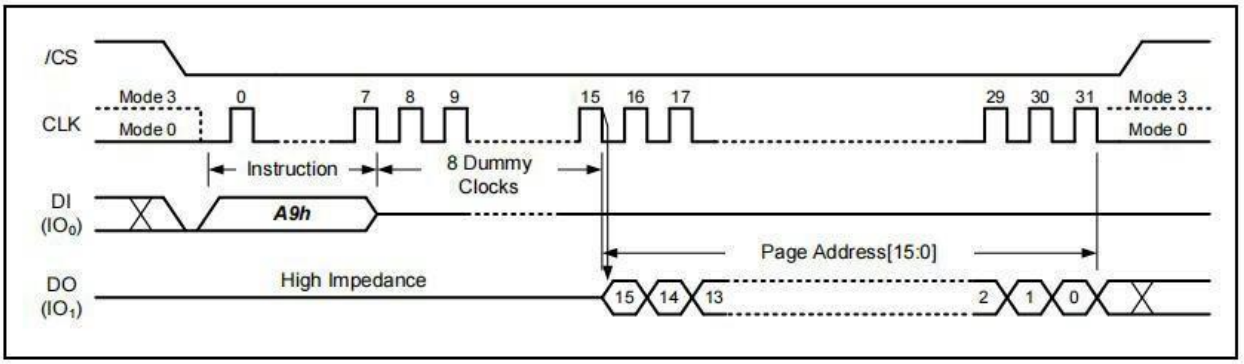
13.4 Last ECC Failure Page Address (A9h)

When the ECC-E bit in the Status/Configuration Register is set to 1 (also power up default), the internal ECC algorithm is enabled for all Program and Read operations.

During the Read operations, ECC information will be used to verify the data read out from the physical memory array and possible corrections can be made to limited amount of data bits that contain errors. The ECC Status Bits (ECC-1 & ECC-0) will also be set indicating the result of ECC calculation.

The ECC failure page address (or the last page address if it‘s multiple pages) can be obtained by issuing the –Last ECC failure Page Address‖ command. The 16-bits Page Address that contains uncorrectable ECC errors will be presented on the DO pin following the instruction code –A9h‖ and 8-bits dummy clocks on the DI pin.

Figure 13-3.Read Last ECC Failure Page Address Timing Diagram



14 Deep Power-down

14.1 Deep Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code –B9hll.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-down instruction will not be executed. After /CS is driven high, the deep power-down state will entered within the time duration of tDP (See AC Characteristics).

While in the deep power-down state only the Release Deep Power-down (ABh) and Reset (FFh) instructions, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring almost instructions makes the Deep Power-down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

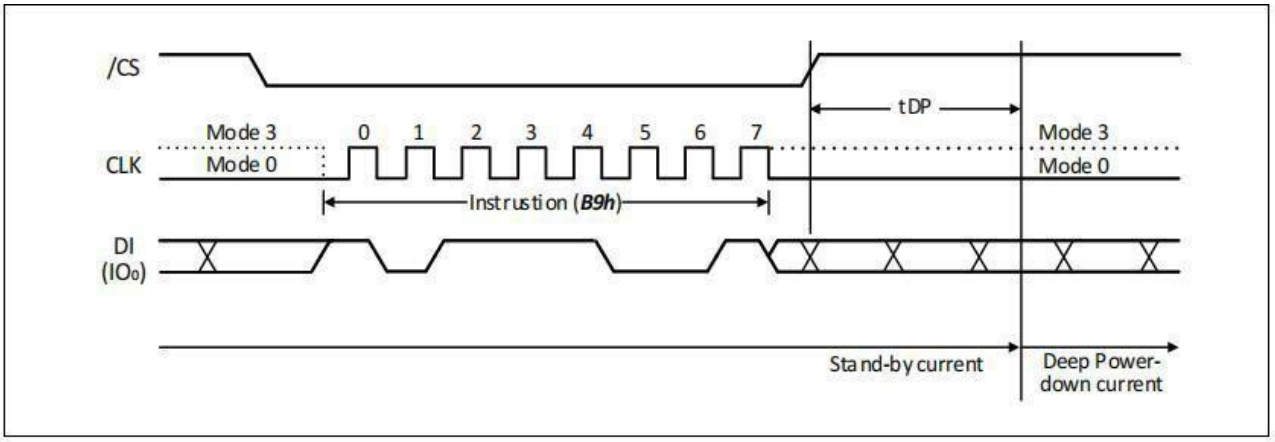


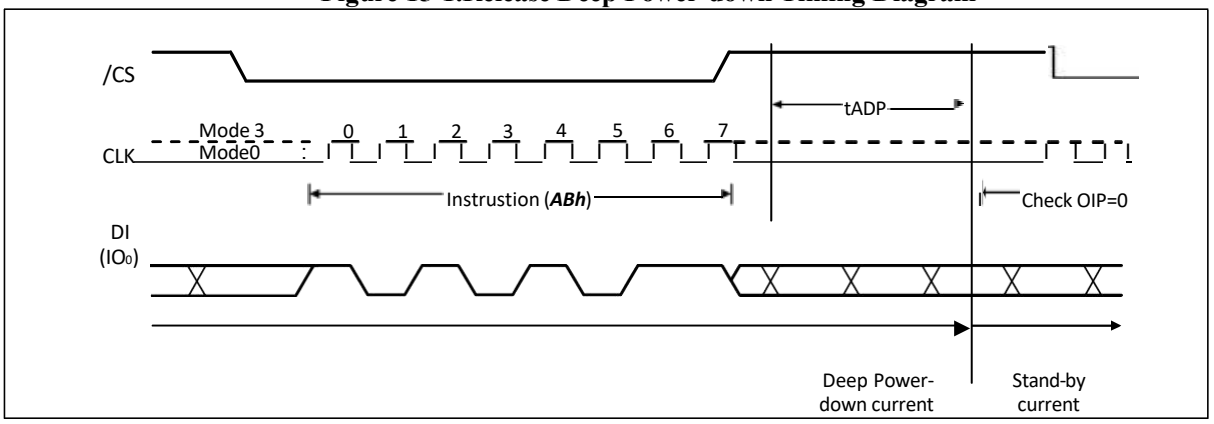
Figure 15-1.Deep Power-down Timing Diagram

14.2 Release Deep Power-down (ABh)

The Release Deep Power-down instruction can be used to release the device from the power-down state. To release the device from the deep power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code –ABhll and driving /CS high. Release from deep power-down state will take the time duration of tADP (See AC Characteristics) before the device will resume normal operation and other instructions are accepted.

To confirm spi-nand actually awake from Deep Power-down, we suggest reading status until OIP=0,just like power-up cycle.

Figure 15-1.Release Deep Power-down Timing Diagram



Symbol	Parameter	Min	Max	Unit
tDP	CS high to enter deep power-down	20		us
tADP	CS high to quit deep power-down	40		us

15 POWER ON TIMING

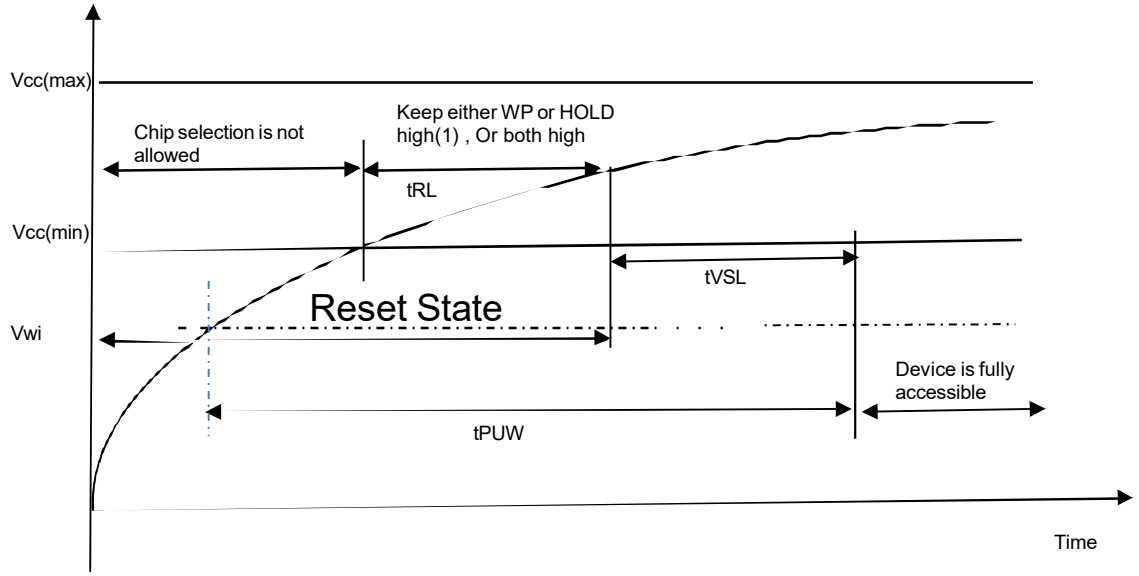


Figure13-1.Power on Timing Sequence

Table 13-1.Power-On Timing and Write Inhibit Threshold for 3.3V

Symbol	Parameter	Min	Max	Unit
Vcc(min)		2.7		V
Vcc(max)			3.6	V
VWI	Write Inhibit Voltage		2.5	V
tRL(1)	Time of keeping either WP or HOLD high, Or both high	800		us
tVSL	Vcc(min) To CS# Low	1.5	2	ms
tPUW	Time Delay From VCC(WI) To Write Instruction	2.5		ms

Note:

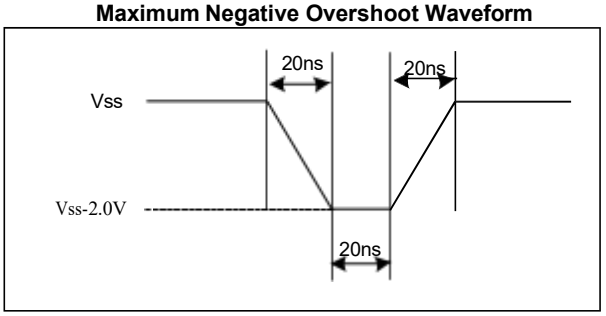
1. After Vcc reach Vcc(min), to release reset state, host should keep either WP or HOLD high for the time of tRL at last. Or reset command(FFH) can also release reset state.

16 ABSOLUTE MAXIMUM RATINGS

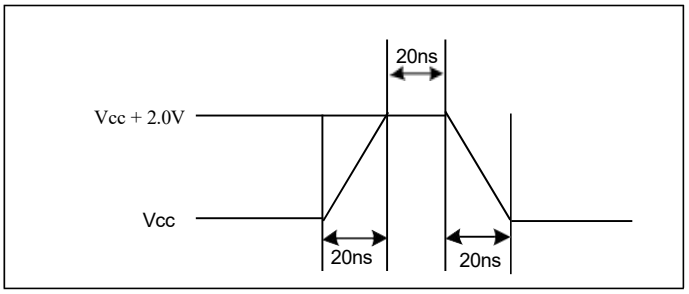
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-45 to 105	℃
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
VCC(3.3V)	-0.6 to 4.0	V

Figure14-1. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



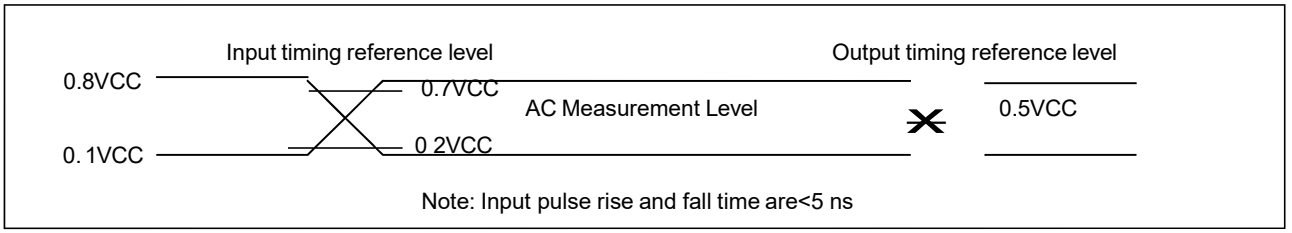
Maximum Positive Overshoot Waveform



17 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 15-1. Input Test Waveform and Measurement Level



18 DC CHARACTERISTIC

(T= -40℃~85℃/-40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current (CMOS) for 45℃	CS#=VCC, V_{IN}=VCC or VSS		65		μA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)			28	mA
I_{CC3}	Operating Current (Program)				30	mA
I_{CC4}	Operating Current (Erase)				30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note: Value guaranteed by design and/or characterization, not 100% tested in production

19 AC CHARACTERISTICS

(T= -40℃~85℃/-40℃~105℃, VCC=2.7~3.6V, C_L=30pF)

Symbol	Parameter	3.3V		Unit.
		Min.	Max.	
FC1	Serial Clock Frequency		104	MHz
tCH	Serial Clock High Time	4		ns
tCL	Serial Clock Low Time	4		ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2		V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2		V/ns
tCHSH	CS# Active Hold Time	5		ns
tSHCH	CS# Not Active Setup Time	5		ns
tSLCH	CS# Active Setup Time	5		ns
tCHSL	CS# Not Active Hold Time	5		ns
tSHSL/tCS	CS# High Time	20		ns
tSHQZ	Output Disable Time		20	ns
tCLQX	Output Hold Time	2		ns
tDVCH	Data In Setup Time	2		ns
tCHDX	Data In Hold Time	2		ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5		ns
tHHCH	Hold# High Setup Time (relative to Clock)	5		ns
tCHHL	Hold# High Hold Time (relative to Clock)	5		ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5		ns
tHLQZ	Hold# Low To High-Z Output		15	ns
tHHQX	Hold# High To Low-Z Output		15	ns
tCLQV	Clock Low To Output Valid		9	ns
tWHSL	WP# Setup Time Before CS# Low	20		ns
tSHWL	WP# Hold Time After CS# High	100		ns
tHODLY	Clock High To Output Valid When HSOD=1	2	7	ns

Note:

1. Value guaranteed by design and/or characterization, not 100% tested in production

20 PERFORMANCE AND TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRST	CS# High To Next Command After Reset(FFh)			500	us
tRD	Read From Array			380	us
tRD_ECC	Read From Array with ECC		380		us
tPROG	Page Programming Time		600		us
tPROG_ECC	Page Programming Time with ECC		400	600	us
tBERS	Block Erase Time		3	5	ms
tPCBSY	Cache busy time for cache Program		20		us
tRCBSY	Cache busy time for cache Read		20		us

Figure 18-1.Serial Input Timing

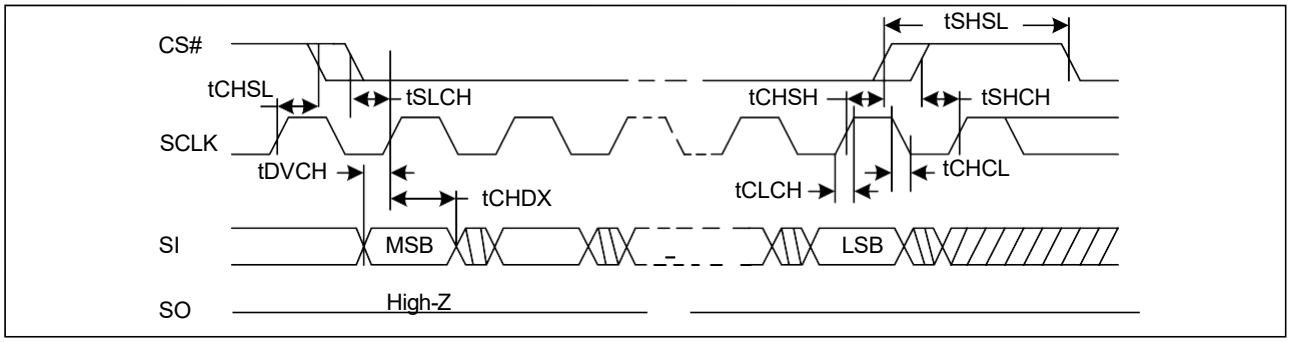


Figure 18-2.Output Timing

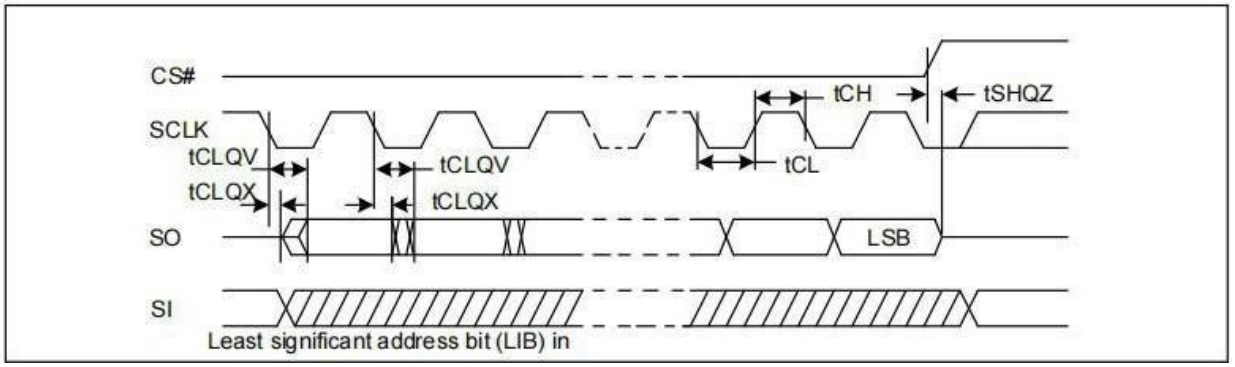


Figure 18-3.Output Timing(HSOD=1)

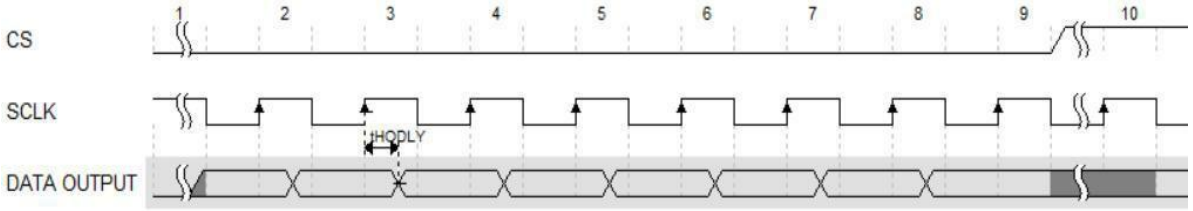
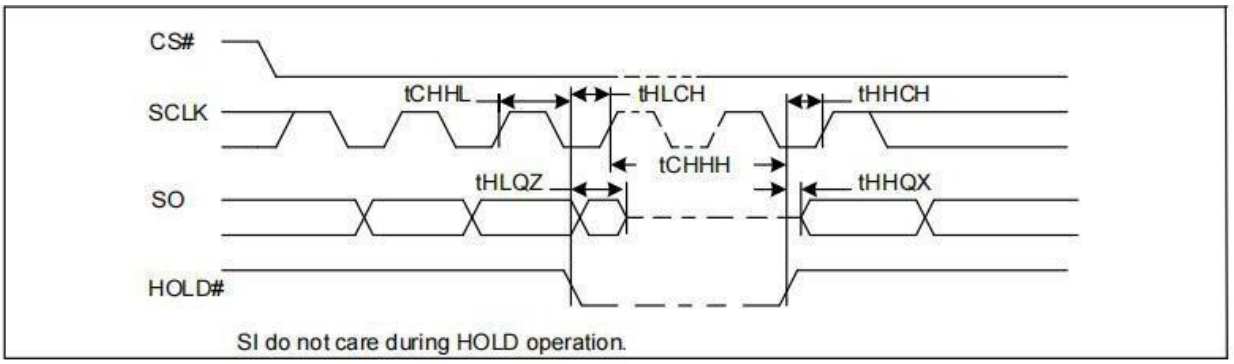
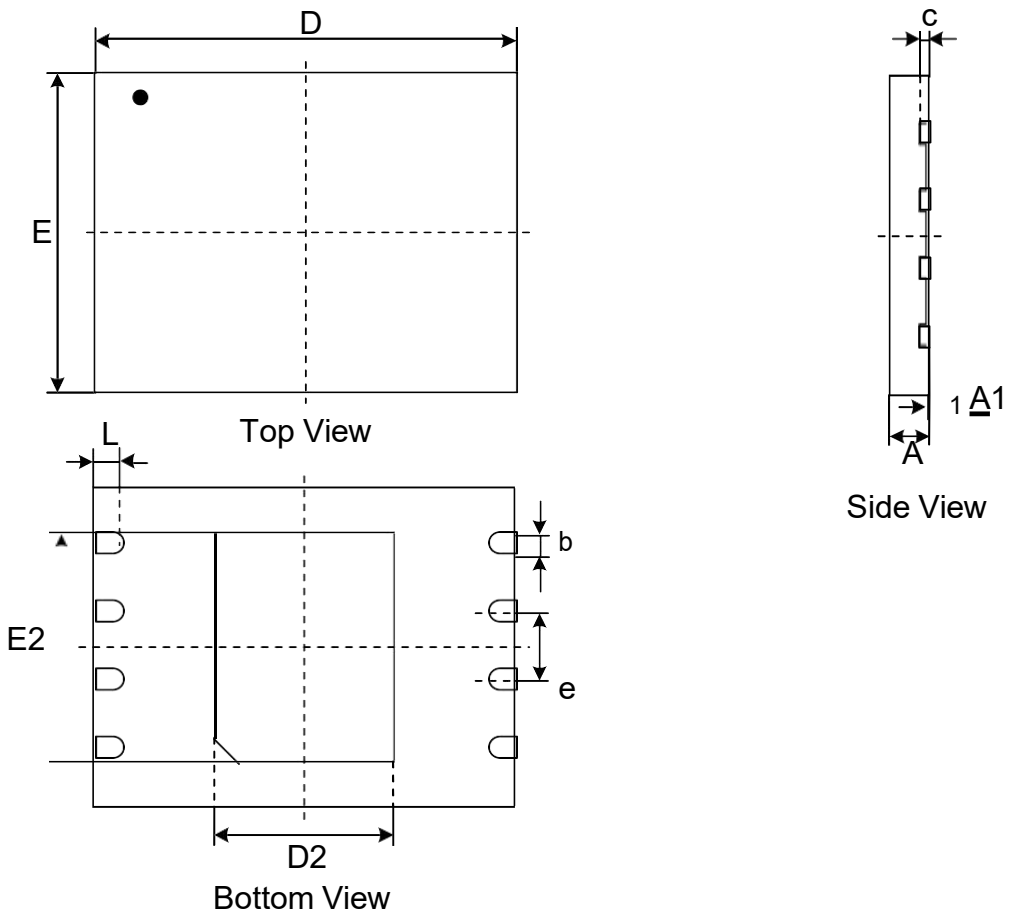


Figure 18-4.Hold Timing



2 PACKAGE INFORMATION

Figure 20-1 LGA8 6.0*8.0mm



Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022