UMW STD15NF10L

100V N-Channel MOSFET

1.Description

The STD15NF10L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge andoperation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

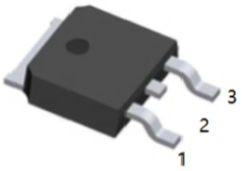
2.Features

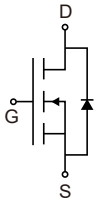
- $V_{DS\ (V)}$=100V
- I_D=20A
- $R_{DS(ON)}$<75mΩ(V_{GS}=10V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK) top view





4.Absolute Maximum Ratings T_C= 25°C

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current, V_{GS}=10V[1]	T_C=25°C	I_D	20	A
	T_C=100°C		10	
Pulsed Drain Current [2]		I_{DM}	30	
Single Pulse Avalanche Energy [3]		E_{AS}	36.5	mJ
Avalanche Current		I_{AS}	15	A
Total Power Dissipation [4]	T_C=25°C	P_D	34.7	W
Storage Temperature Range		T_{STG}	-55 to 150	°C
Junction Temperature Range		T_J	-55 to 150	°C
Thermal Resistance Junction-ambient [1]		$R_{\theta JA}$	62	°C/W
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	2.4	°C/W

6.T_J=25°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
BV_{DSS} Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D=1mA,Reference to 25°C		0.098		V/°C
Static Drain-to-Source On-Resistance [2]	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		65	75	mΩ
		V_{GS}=4.5V, I_D=15A		85	90	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		2.5	V
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA		-4.75		mV/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V, T_J=25°C			10	μA
		V_{DS}=80V, V_{GS}=0V, T_J=55°C			100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=20A		28.7		S
Gate Resistance	R_g	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.6	3.2	Ω
Total Gate Charge (10V)	Q_g	V_{DS}=80V, V_{GS}=10V, I_D=20A		26.2		nC
Gate-Source Charge	Q_{gs}			4.6		nC
Gate-Drain Charge	Q_{gd}			5.1		nC
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=50V, V_{GS}=10V, R_G=3.3Ω, I_D=20A		4.2		ns
Rise Time	t_r			8.2		ns
Turn-Off Delay Time	$t_{D(off)}$			35.6		ns
Fall Time	t_f			9.6		ns
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		1535		pF
Output Capacitance	C_{oss}			60		pF
Reverse Transfer Capacitance	C_{rss}			37		pF
Continuous Source Current [1,5]	I_S	V_G=V_D=0V, Force Current			22	A
Pulsed Source Current [2,5]	I_{SM}				30	A
Diode Forward Voltage [2]	V_{SD}	V_{GS}=0V, I_S=1A, T_J=25°C			1.2	V
Reverse Recovery Time	t_{rr}	I_F=20A, dI/dt=100A/μs, T_J=25°C		30		ns
Reverse Recovery Charge	Q_{rr}			37		nC

Note :

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.

3.The E_{AS} data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=27A.

4.The power dissipation is limited by 150°C junction temperature.

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

7.1Typical Characterisitics

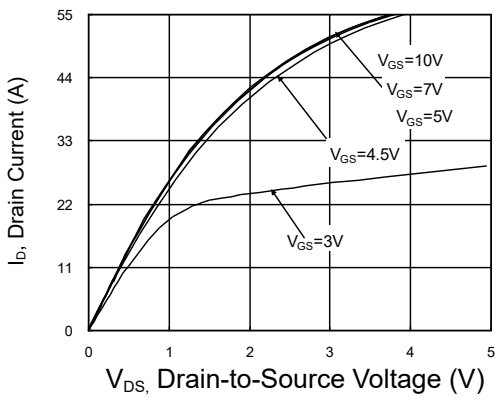


Figure 1: Typical Output Characteristics.

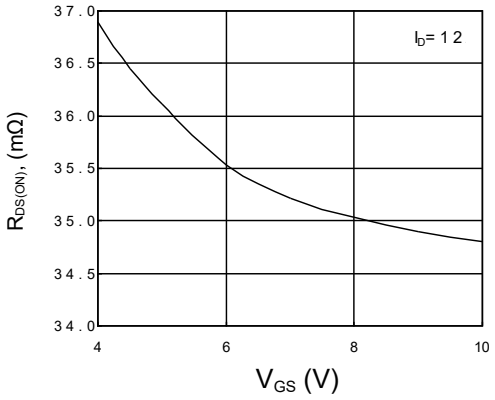


Figure 2: On-Resistance vs. G-S Voltage.

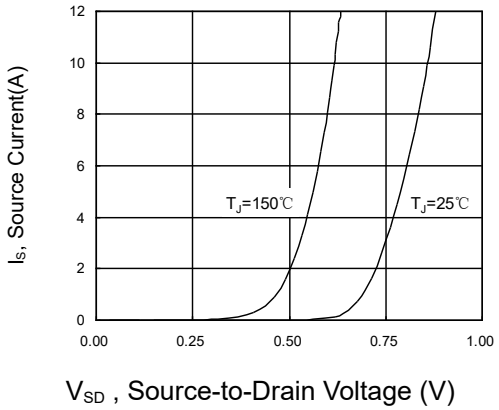


Figure 3: Forward Characteristics of Reverse.

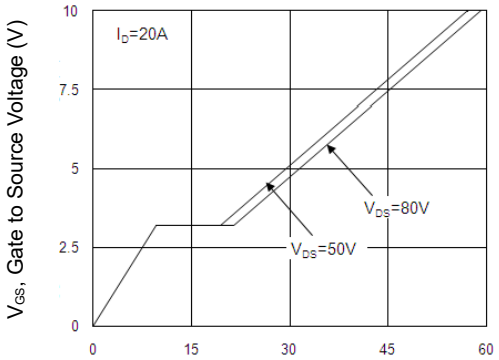


Figure 4: Gate-charge Characteristics.

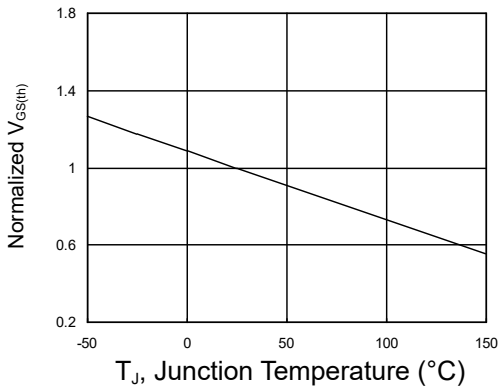


Figure 5: Normalized $V_{GS(th)}$ vs. T_J.

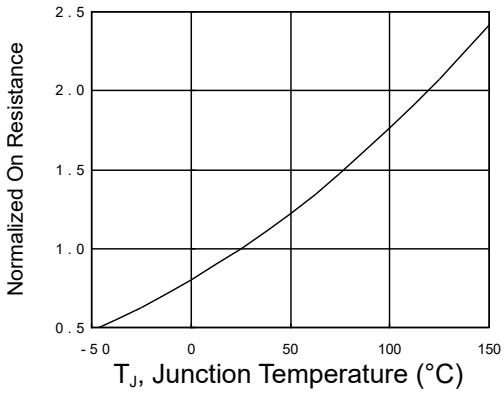


Figure 6: Normalized $R_{DS(ON)}$ vs. T_J.

7.2Typical Characterisitics

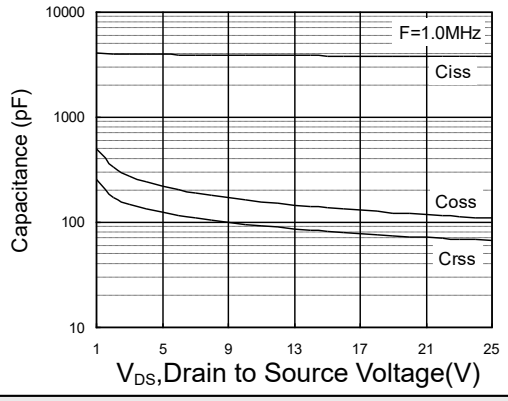


Figure 7: Capacitance.

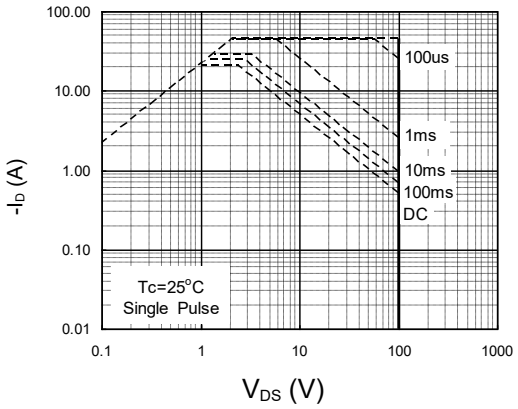


Figure 8: Safe Operating Area.

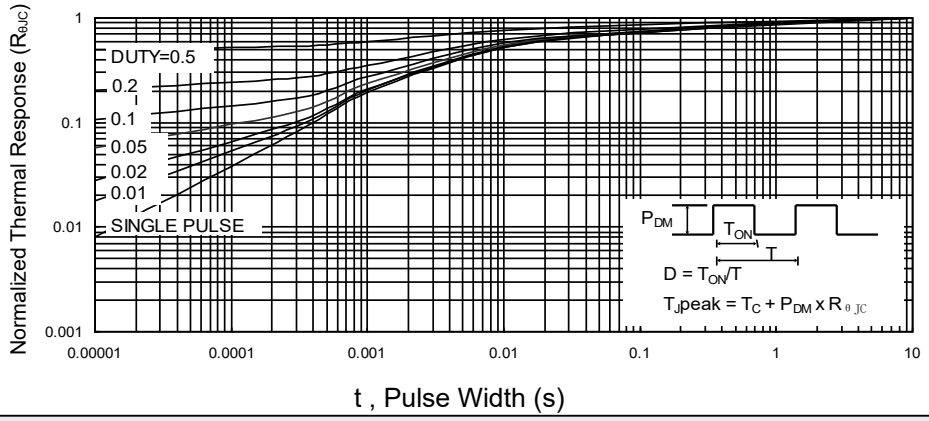


Figure 9: Normalized Maximum Transient Thermal Impedance.

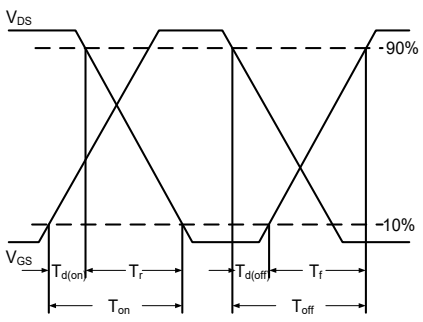


Figure 10: Switching Time Waveform

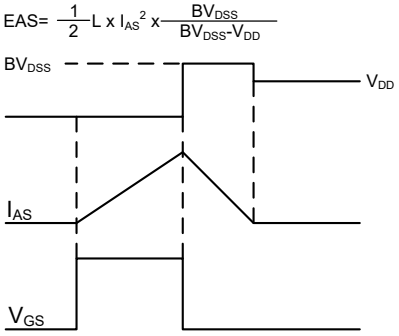
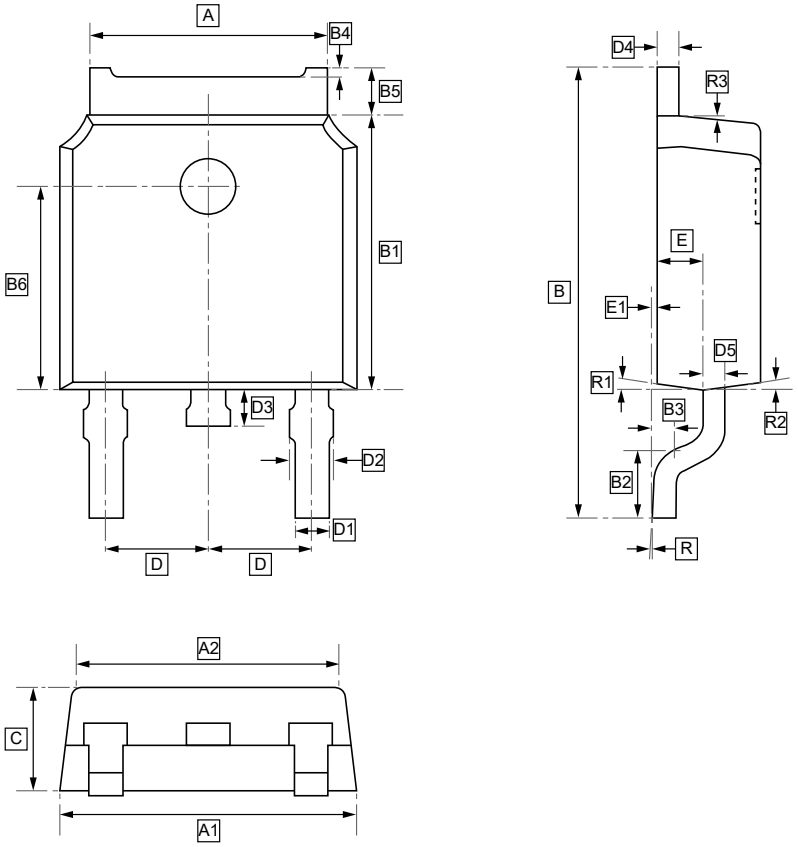


Figure 11: Unclamped Inductive Waveform

8.TO-252 Package Outline Dimensions

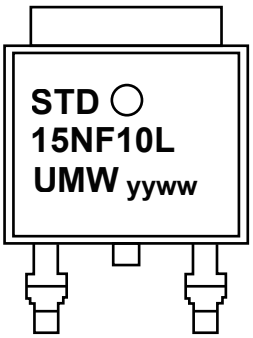


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	B3	B4	B5	B6	C	D
Min	5.1	6.4	5.6	9.5	5.9	1.35	0.4	0.1	0.85	4.35	2.15	2.286
Max	5.5	6.8	6.0	10.3	6.3	1.65	0.6	(typ.)	1.05	4.65	2.45	(typ.)

Symbol	D1	D2	D3	D4	D5	E	E1	R	R1	R2	R3
Min	0.66	0.81	0.65	0.42	0.42	0.86	0.05	0°	7°	7°	7°
Max	0.86	1.01	0.95	0.58	0.58	1.16	0.05	6°	(typ.)	(typ.)	(typ.)

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW STD15NF10L	TO-252	2500	Tape and reel

10.Disclaimer

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