UMW FDS3672

100V N-Channel MOSFET

1.Features

- V_{DS}=100V
- I_D=7.5A
- $R_{DS(ON)}$=19mΩ(V_{GS}=10V)
- Q_g(tot) = 28nC(Typ.),V_{GS}=10V
- Low Miller Charge
- Low Q_{rr} Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

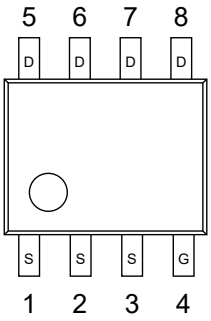
2.Applications

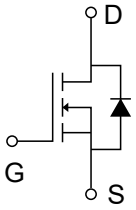
- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GS}	±20	
Drain Current Continuous (T_A=25°C, V_{GS}=10V, $R_{\theta JA}$=50°C/W)	I_D	7.5	A
Continuous (T_A=100°C, V_{GS}=10V, $R_{\theta JA}$=50°C/W)		4.8	
Pulsed		Figure 4	
Single Pulse Avalanche Energy (Note 1)	E_{AS}	416	mJ
Power Dissipation	P_D	2.5	W
Derate above 25°C		20	mW/°C
Operating and Storage Temperature	T_J,T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	$R_{\theta JA}$	85	°C/W
Thermal Resistance, Junction to Case (Note 2)	$R_{\theta JC}$	25	°C/W

6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V			1	μA
		T_C=150°C			250	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V			±100	nA
On Characteristics						
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2		4	V
Drain to Source On Resistance	$R_{DS(ON)}$	I_D=7.5A, V_{GS}=10V		19	23	mΩ
		I_D=6.8A, V_{GS}=6V		24	28	mΩ
		I_D=7.5A, V_{GS}=10V, T_C=150°C		35	43	mΩ
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=25V		2015		pF
Output Capacitance	C_{oss}	V_{GS}=0V		285		pF
Reverse Transfer Capacitance	C_{rss}	f=1MHz		70		pF
Total Gate Charge at 10V	Q_g(TOT)	V_{GS}=0V to 10V		28	37	nC
Threshold Gate Charge	Q_g(TH)	V_{GS}=0V to 2V		4	6	nC
Gate to Source Gate Charge	Q_{gs}	V_{DD}=50V		10		nC
Gate Charge Threshold to Plateau	Q_{gs2}	I_D=7.5A		6.8		nC
Gate to Drain “Miller” Charge	Q_{gd}	I_G=1mA		6		nC
Switching Characteristics (V_{GS}=10V)						
Turn-On Time	t_{ON}	V_{DD}=50V, I_D=4A V_{GS}=10V, R_{GS}=10Ω			51	ns
Turn-On Delay Time	$t_{D(on)}$			14		ns
Rise Time	t_r			20		ns
Turn-Off Delay Time	$t_{D(off)}$			37		ns
Fall Time	t_f			27		ns
Turn-Off Time	t_{OFF}				96	ns

Drain-Source Diode Characteristics						
Source to Drain Diode Voltage	V_{SD}	I_{SD}=7.5A			1.25	V
		I_{SD}=4A			1	V
Reverse Recovery Time	t_{rr}	I_{SD}=7.5A, dI_{SD}/dt=100A/μs			55	ns
Reverse Recovered Charge	Q_{rr}	I_{SD}=7.5A, dI_{SD}/dt=100A/μs			90	nC

Notes:

1: Starting T_J=25°C, L=13mH, I_{AS}= 8A.

2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

3: $R_{\theta JA}$ is measured with 1.0 in2 copper on FR-4 board

7.1 Typical Characteristic

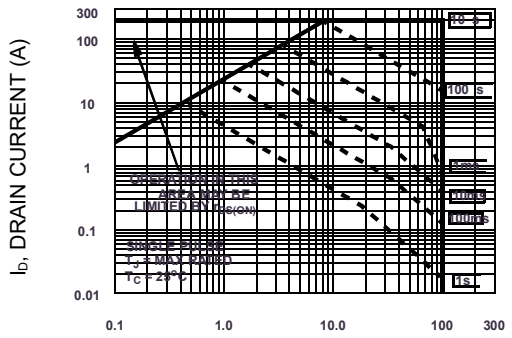


Fig 1: Forward Bias Safe Operating Area

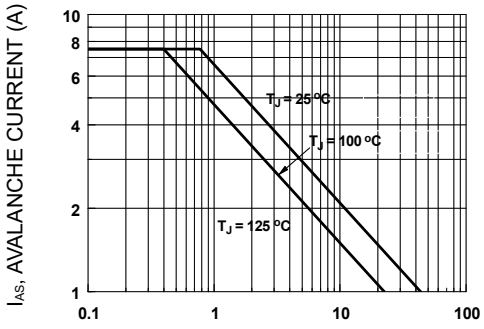


Figure 2: Unclamped Inductive Switching Capability

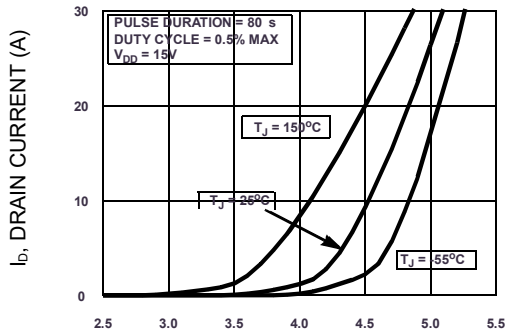


Figure 3: Transfer Characteristics

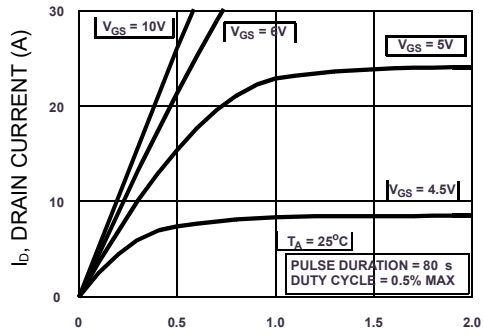


Figure 4: Saturation Characteristics

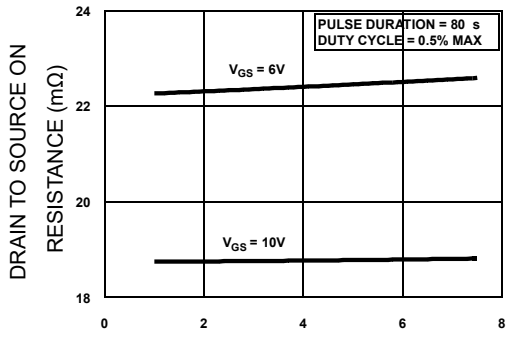


Figure 5: Drain to Source On Resistance vs Drain Current

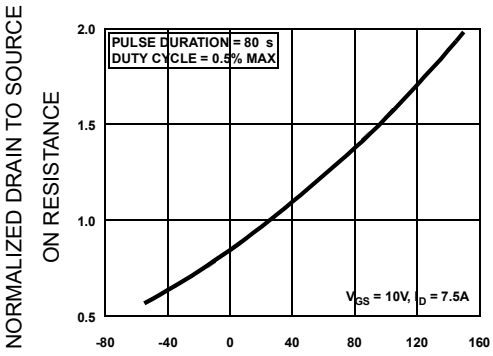
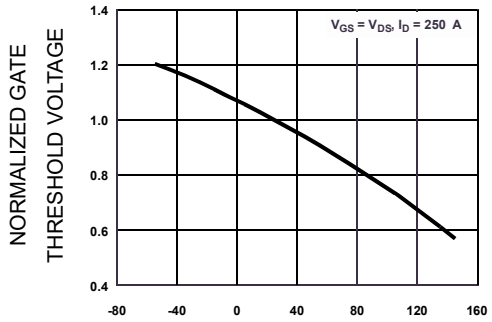


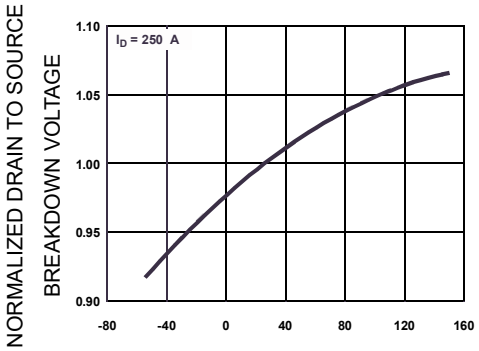
Figure 6: Normalized Drain to Source On Resistance vs Junction Temperature

7.2 Typical Characteristic



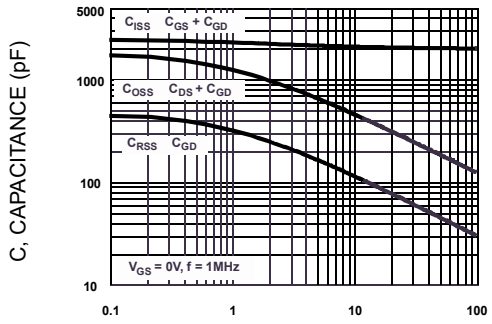
T_J, JUNCTION TEMPERATURE (°C)

Figure 6: Normalized Drain to Source On Resistance vs Junction Temperature



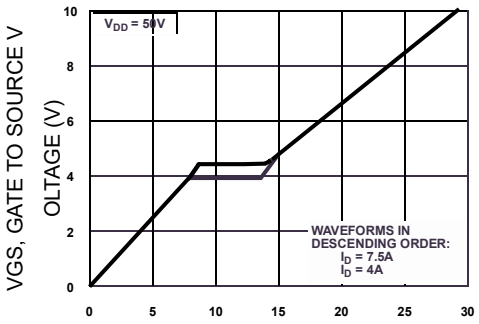
T_J, JUNCTION TEMPERATURE (°C)

Figure 2: Normalized Drain to Source Breakdown Voltage vs Junction Temperature



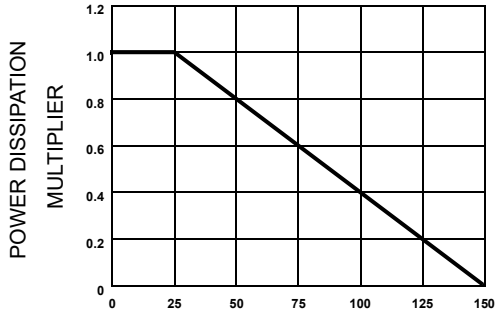
V_{DS}, DRAIN TO SOURCE VOLTAGE (V)

Figure 3: Capacitance vs Drain to Source Voltage



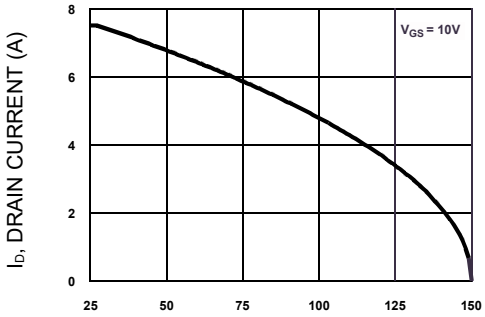
Q_g, GATE CHARGE (nC)

Figure 4: Gate Charge Waveforms for Constant Gate Currents



T_A, AMBIENT TEMPERATURE (°C)

Figure 5: Normalized Power Dissipation vs Ambient Temperature



T_C, CASE TEMPERATURE (°C)

Figure 6: Maximum Continuous Drain Current vs Case Temperature

7.3 Typical Characteristic

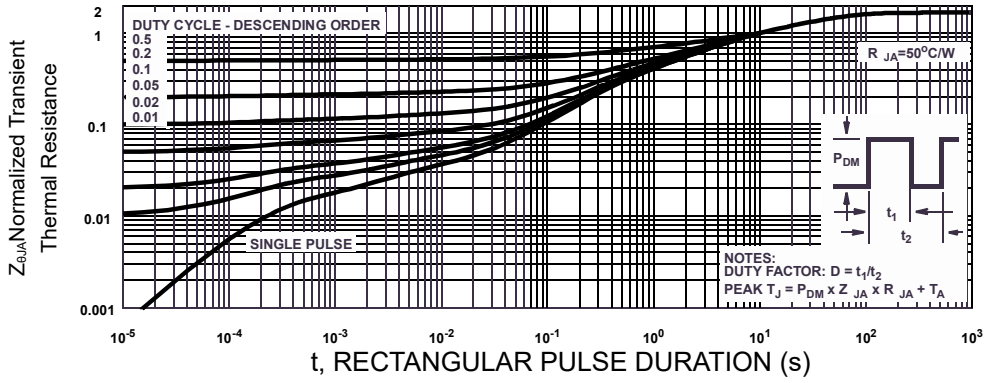


Figure 12: Normalized Maximum Transient Thermal Impedance

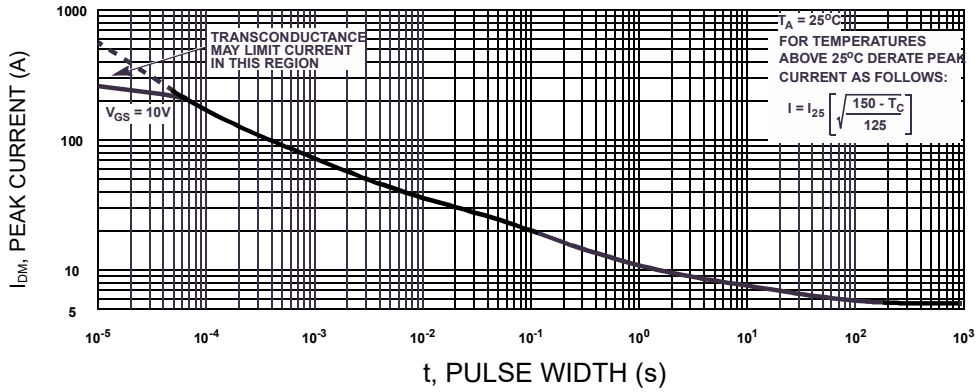
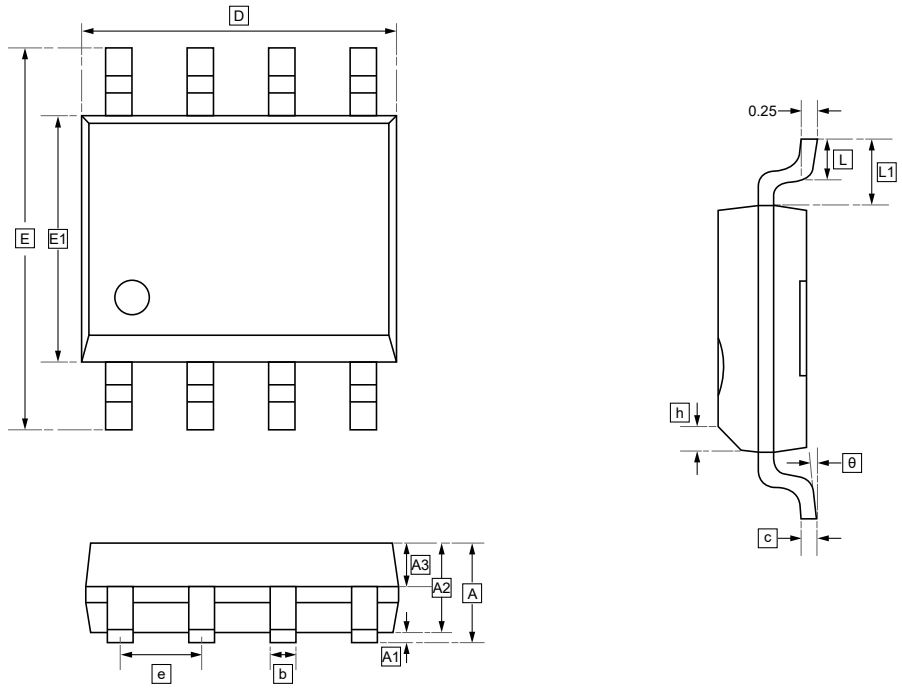


Figure 12: Peak Current Capability

8.SOP-8 Package Outline Dimensions

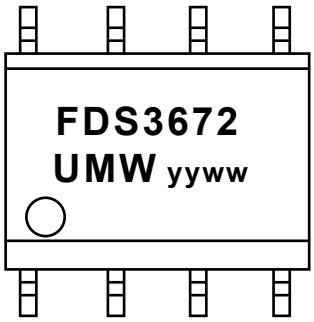


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS3672	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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