UMW IRF7103TR

50V N-Channel MOSFET

1.Description

The SOP-8 has been modified through a customized leadframe for enhanced thermal characteristics and dual-die capability making it ideal in a variety of power applications.With these improvements, multiple devices can be used in an application with dramatically.

2.1Features

- $V_{DS\ (V)}$=50V
- I_D=3A
- $R_{DS(ON)}$<0.09Ω(V_{GS}=10V)
- $R_{DS(ON)}$<0.14Ω(V_{GS}=4.5V)

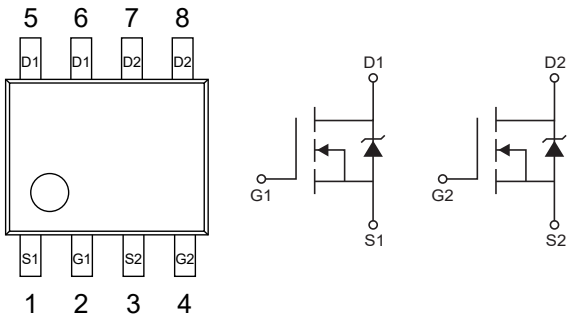
2.2Features

- Adavanced Process Technology
- Ultra Low On-Resistance
- Surface Mount
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

3.Pinning information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS}=10V	T_A=25°C	I_D	3	A
Continuous Drain Current, V_{GS}=10V	T_A=100°C		2.3	A
Pulsed Drain Current ①		I_{DM}	10	A
Power Dissipation	T_A=25°C	P_D	2	W
Linear Derating Factor			0.016	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Peak Diode Recovery dv/dt ②		dv/dt	4.5	V/nS
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$		62.5	°C/W

6.Electrical Characteristics T_J=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	50			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	I_D=1mA,Reference to 25°C		0.049		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3A ③		0.07	0.09	Ω
		V_{GS}=4.5V, I_D=1.5A ③		0.11	0.14	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		3	V
Forward Transconductance	g_{FS}	V_{DS}=15V, I_D=3A ③		3.8		S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V			2	μA
		V_{DS}=40V,V_{GS}=0V,T_J=55°C			25	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=20V			100	nA
Gate-to-Source Reverse Leakage		V_{GS}=-20V			-100	
Total Gate Charge	Q_g	I_D=2A		12	30	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=25V		1.2		
Gate-to-Drain ("Miller") Charge	Q_{gd}	V_{GS}=10V ③		3.5		
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=25V		9	20	ns
Rise Time	t_r	I_D=1A		8	20	ns
Turn-Off Delay Time	$t_{D(off)}$	R_G=6Ω		45	70	ns
Fall Time	t_f	R_D=25Ω ③		25	50	ns
Internal Drain inductance	L_D	Between lead,6mm (0.25in.) from package and centerof die contact		4		nH
Internal Source inductance	L_S			6		
Input Capacitance	C_{iss}	V_{GS}=0V		290		pF
Output Capacitance	C_{oss}	V_{DS}=25V		140		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz		37		pF

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			2	A
Pulsed Source Current (Body Diode) ①	I_{SM}				12	
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=1.5A,V_{GS}=0V③			1.2	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=1.5A		70	100	ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/μs ③		110	170	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited bymax.junction temperature.

② I_{SD}≤ 1.8A, di/dt ≤ 90A/μS, V_{DD}≤ $V_{(BR)DSS}$,T_J≤ 150°C.

③ Pulse width ≤ 300us; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 10sec.

7.1Typical Characterisitics

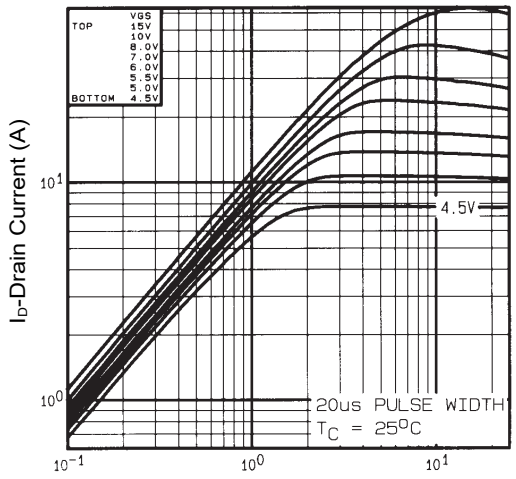


Fig 1. Typical Output Characteristics

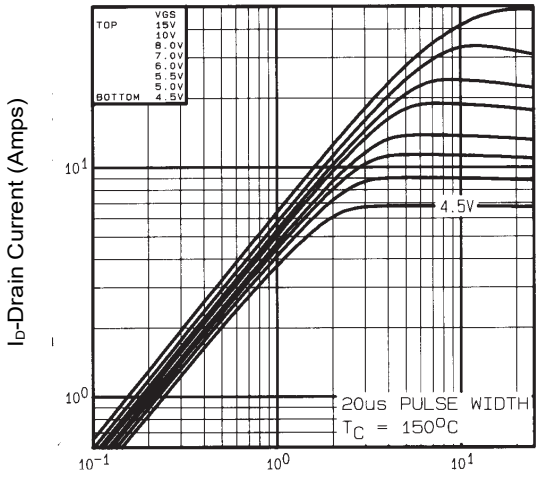


Fig 2. Typical Output Characteristics

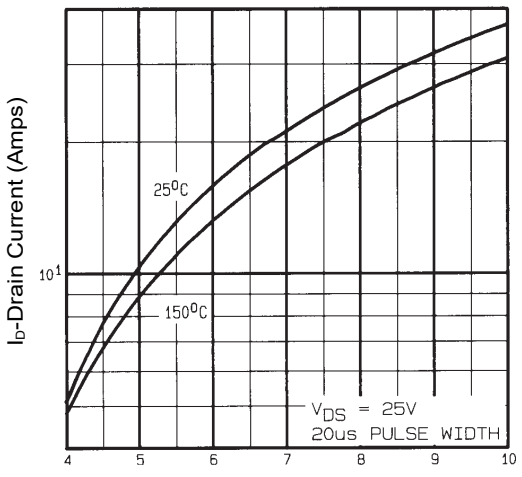


Fig 3. Typical Transfer Characteristics

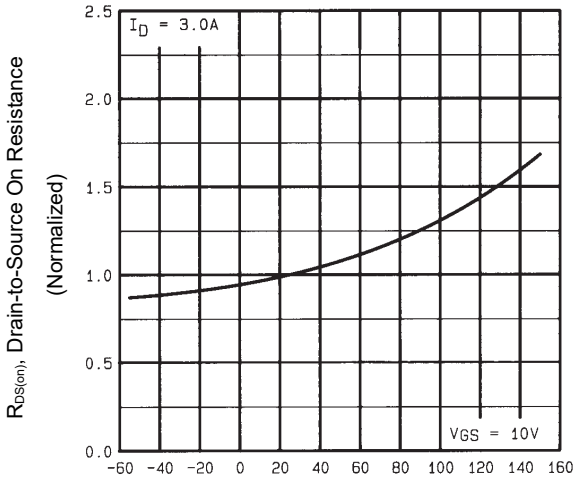
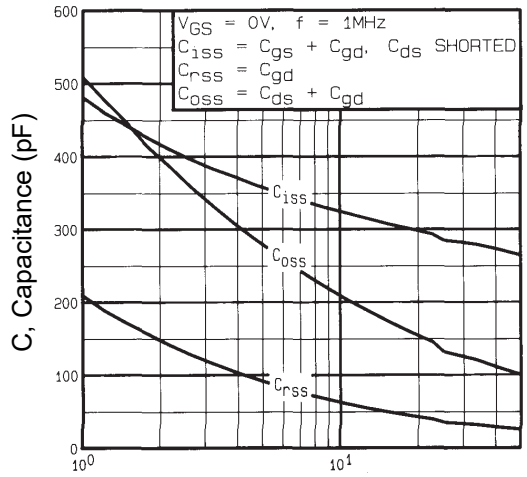


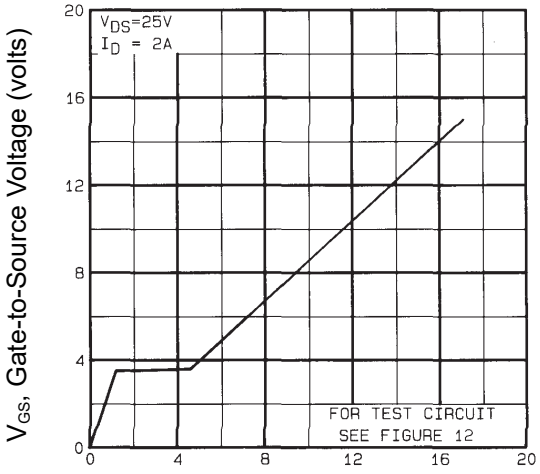
Fig 4. Nomalized On-ResistanceVs. Temperature

7.2Typical Characterisitics



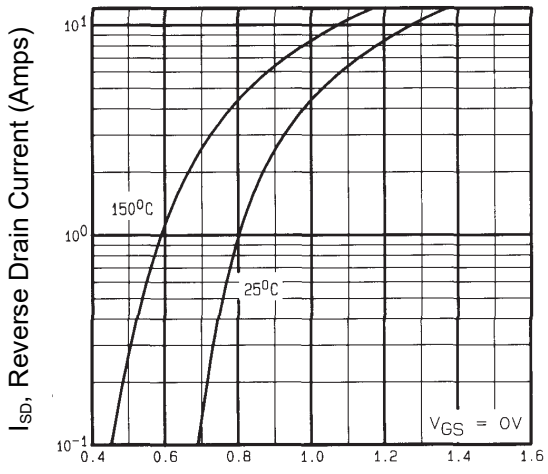
V_{DS} ,Drain-to-Source Voltage (V)

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage



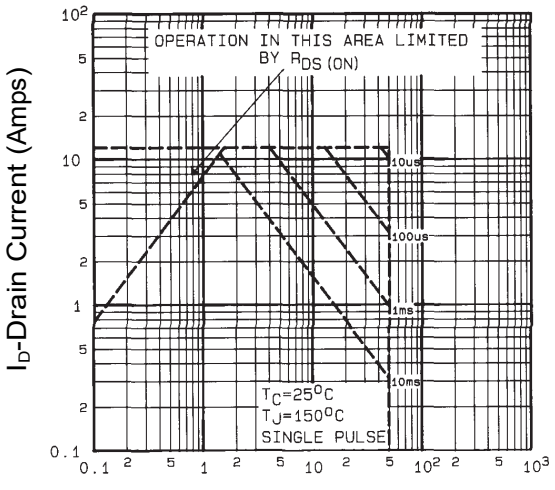
Q_G, Total Gate Charge (nC)

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



V_{SD}, Source-to-Drain Voltage (volts)

Fig 7. Typical Source-Drain Diode Forward Voltage



V_{DS}, Drain-to-Source Voltage (volts)

Fig 8. Maximum Safe Operating Area

7.3Typical Characterisitics

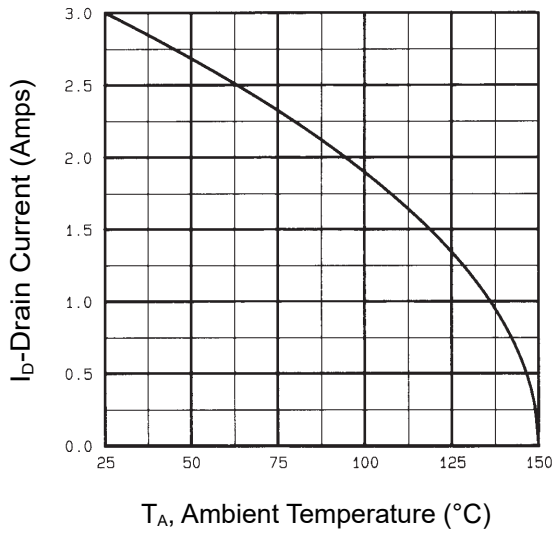


Fig 9. Maximum Drain Current Vs.AmbientTemperature

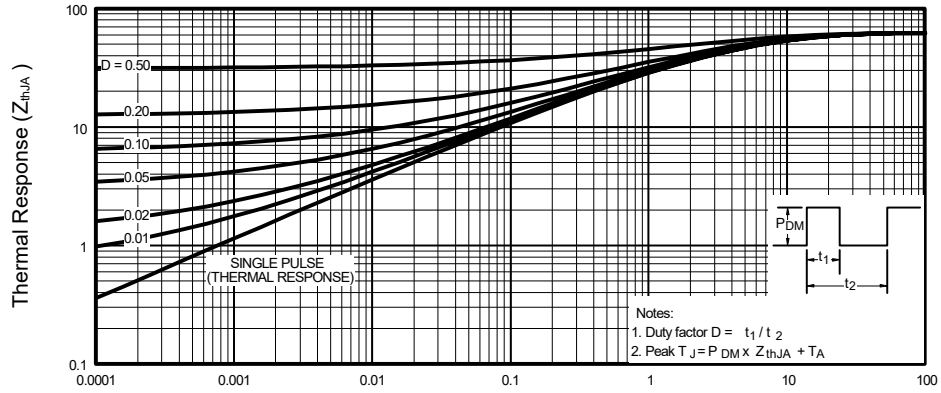


Fig 10. Maximum Effective Transient Themal Impedance, Junction-to-Ambient

7.4Typical Characterisitics

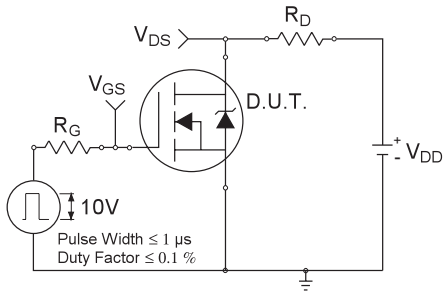


Fig 11a. Switching Time Test Circuit

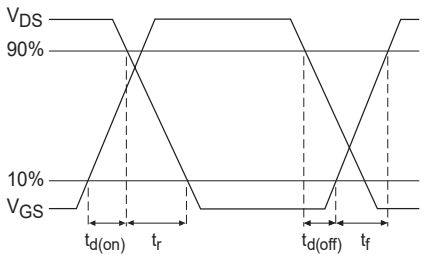


Fig 11b. Switching Time Waveforms

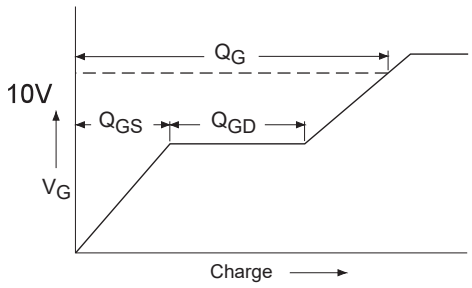


Fig 12a. Basic Gate Charge Waveform

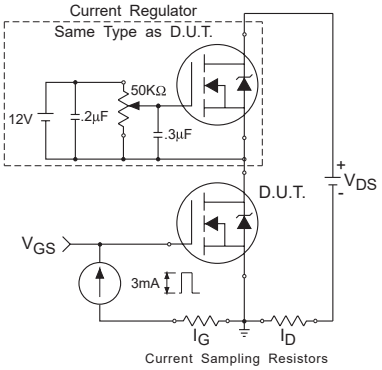
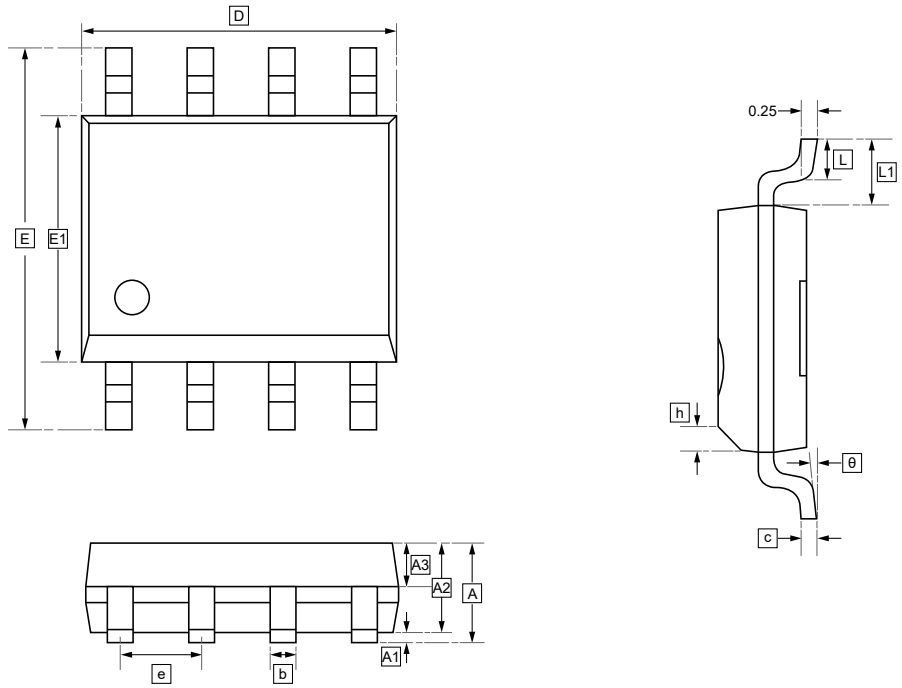


Fig 12b. Gate Charge Test Circuit

8.SOP-8 Package Outline Dimensions

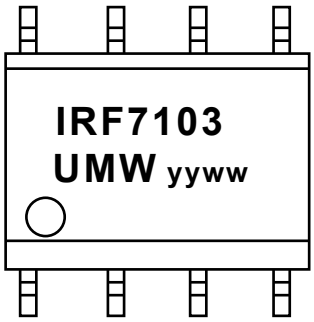


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7103TR	SOP-8	3000	Tape and reel

10.Disclaimer

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